High-performance Sub-1GHz RF Transceiver

Features

- Frequency range: 113 – 960 MHz
- Modulation/demodulation: OOK, 2 (G)FSK, 4 (G)FSK
- Data rate: 0.1 - 1000 kbps
- Sensitivity: 2 FSK, -122 dBm DR=2.4 kbps, 433.92 MHz
  4 FSK, -88 dBm DR=1 Mbps,433.92 MHz
  OOK, -94 dBm DR= 300 kbps, 433.92 MHz
- Adjacent channel rejection : 62 dBc, BW = 4.8 kHz,
  Channel space = 12.5 kHz
- Blocking: 76 dBc , ±1 MHz offset, BW = 4.8 kHz
- Operating voltage range: 1.8 - 3.6 V
- Tx current: 30 mA @ 13 dBm, 433.92 MHz, FSK
  82 mA @ 20 dBm, 433.92 MHz, FSK
- Rx current: 9.6 mA (DCDC) @433.92 MHz, FSK
- No extra RF switching components required in single antenna mode
- Multiple super-low power (SLP) Rx modes available
- Sleep current
  - 400 nA, Duty Cycle = OFF
  - 800 nA, Duty Cycle = ON
- Special features:
  - Quick and stable automatic frequency control (AFC)
  - 3 varied clock data recovery systems (CDR)
  - Quick and accurate valid signal detection (PJD, RSSI)
  - Super-low power (SLP) and Duty Cycle receiving
  - Fast Tx or Rx frequency hopping
  - Carrier sense multiple access (CSMA)
  - Automatic ACK and re-sending
  - Antenna diversity
- 4-wire SPI interface
- Supporting both direct and packet modes, with configurable packet handler and 128-Byte FIFO
- NRZ format, Manchester, whiten data coding, FEC

Application

- Automatic meter reading
- Home security and building automation
- ISM-band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor node
- Tag reader and writer

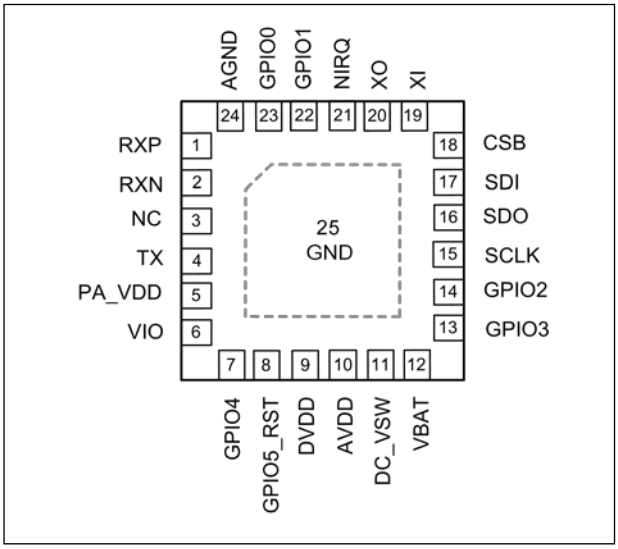
Ordering Information

Product Model	Frequency	Package	Minimum Order
CMT2310A-EQR	113 - 960 MHz	QFN24	3,000 pcs
Refer to Table 22 for more ordering information.			

QF24 (4X4)

Description

The CMT2310A is an ultra-low power, high-performance, OOK / 2(G)FSK / 4(G)FSK based RF transceiver, applicable to various applications within the 113 - 960 MHz frequency band. The product is part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers and transceivers. The high-density integration of CMT2310A simplifies the required BOM in system design. With Tx power reaching +20 dBm and sensitivity reaching -122 dBm, it can achieve optimized performance of application RF links. Through providing multiple data packet formats and code methods, this product ensures the flexible supporting of various applications. Besides, the CMT2310A provides functions such as 128-byte Tx/Rx FIFO, multiple GPIO and interrupt configurations, Duty-Cycle mode, LBT (listen before talk), high-precision RSSI, LBD, power on reset, low-frequency clock output, quick frequency hopping, squelch, etc., which allows more flexible application design and gains more product differentiation capability.



CMT2310A Top View

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1 Electrical Specifications

The measurement conditions are: V_{DD}= 3.3 V，T_{OP}= 25 °C，F_{RF} = 433.92 MHz, sensitivity is measured by receiving a PN9 sequence, matching to 50 Ω impedance and 0.1% BER if nothing else stated. All measurement results are obtained using the evaluation board CMT2310A-EM if nothing else stated.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		-0.3	3.6	V
Interface voltage	V_{IN}		-0.3	3.6	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Last for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2310A is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.

Caution! ESD sensitive device.Precaution should be used when handlingthe device in order to prevent performance degradation or loss of functionality.

1.3 RF Power Consumption

Table 3. RF Power Consumption

Parameter	Symbol	Condition	Typ. (Disable DCDC)	Typ. (Enable DCDC)	Unit
Sleep current [1]	I_{SLEEP}	In sleep mode with sleep timer disabled	400		nA

Parameter	Symbol	Condition		Typ. (Disable DCDC)	Typ. (Enable DCDC)	Unit
		In sleep mode with sleep timer enabled		800		nA
Ready current [1]	I_{Ready}			2.1	1.9	mA
RFS current [1]	I_{RFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
TFS current [1]	I_{TFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
RX current [1]	I_{Rx}	DR = 10 kbps Dev =10 kHz	315 MHz	13.5	8.8	mA
			433 MHz	13.6	9.4	mA
			868 MHz	14.3	9.9	mA
			915 MHz	14.3	9.9	mA
TX current [1]	I_{Tx}	20 dBm[2]	315 MHz	74	/	mA
			433 MHz	82	81	mA
			868 MHz	88	87	mA
			915 MHz	88	87	mA
		13 dBm [3]	315 MHz	26.7	/	mA
			433 MHz	30	29	mA
			868 MHz	33	32	mA
			915 MHz	34	33	mA
		10 dBm [3]	315 MHz	21	15	mA
			433 MHz	25	24	mA
			868 MHz	27	26	mA
			915 MHz	27	26	mA
		-10 dBm [3]	315 MHz	10.3	7	mA
			433 MHz	11	10	mA
			868 MHz	12	11	mA
			915 MHz	12	11	mA

Notes:

[1]. 2FSK, DR = 10 kbps, F_{DEV} = 5 kHz, Vbat = 3.3 V.

[2]. Apply 20 dBm matching network.

[3]. Apply 13 dBm matching network.

1.4 Receiver

Table 4. Receiver Specifications

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Data rate	DR	OOK		0.1		300	kbps
		2 (G)FSK		0.1		500	kbps
		4(GFSK		0.1		1000	kbps
Deviation (RX)	F_{DEV}	(G)FSK, 4(G)FSK[1]		0.5		350	kHz
Sensitivity @ 433 MHz (direct tiematching network)	S_{433}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz,BW= 4.8kHz		-122		dBm
			DR = 10 kbps,F_{DEV} = 5 kHz		-114		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-112		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
			DR =100 kbps, F_{DEV} = 50 kHz		-106		dBm

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
			DR =200 kbps, F_{DEV} = 100 kHz		-104		dBm
			DR =500 kbps, F_{DEV} = 250 kHz		-98		dBm
		OOK[2]	5 kbps		-110		dBm
			50 kbps		-101		dBm
			100 kbps		-97		dBm
			200 kbps		-95		dBm
			300 kbps		-94		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10kHz		-109		dBm
			DR = 100 kbps, F_{DEV}[3] =100kHz		-99		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-88		dBm
Sensitivity @ 868 MHz (direct tie matching network)	S_{868}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz, BW=4.8kHz		-120		dBm
			DR = 10 kbps,F_{DEV} = 5 kHz		-111		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-110		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-107		dBm
			DR =100 kbps, F_{DEV} = 50 kHz		-104		dBm
			DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
			DR =500 kbps, F_{DEV} = 250 kHz		-96		dBm
		OOK[2]	5 kbps		-106		dBm
			50 kbps		-98		dBm
			100 kbps		-94		dBm
			200 kbps		-93		dBm
			300 kbps		-92		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10kHz		-106		dBm
			DR = 100 kbps, F_{DEV}[3] = 100kHz		-96		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-85		dBm

Notes:

[1]. BT = 0.5 by default for Gaussian modulation.
[2]. In case of unspecified BW value, a crystal of 10 ppm is used and the BW value is automatically calculated by RFPDK.
[3]. For 4 FSK, F_{DEV} represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.

Receiver channel bandwidth	BW	Receiver channel bandwidth		1.3		1168	kHz
Saturation input signal level	P_{LVL}					20	dBm
RSSI range	RSSI	By a step of 1 dB		-127		20	dBm
Co-channel rejection @ 433 MHz，868 MHz	CCR	DR = 2.4 kbps; FDEV = 1.2 kHz; BW=4.8 kHz CW interference, BER<0.1%			-7		dB
Adjacent channel rejection @ 433 MHz	ACR-I_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW= 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER<0.1%			62		dB
Adjacent channel rejection @ 868 MHz	ACR-I_{868}	DR = 2.4 kbps；F_{DEV} = 1.2 kHz; BW= 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER<0.1%			56		dB
Blocking	BI_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz;	±1 MHz offset		76		dB

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
@ 433 MHz		BW=4.8 kHz, CW interference, BER<0.1%	±2 MHz offset		80		dB
			±10 MHz offset		84		dB
Blocking @ 868 MHz	BI_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW=4.8 kHz, CW interference, BER<0.1%	±1 MHz offset		66		dB
			±2 MHz offset		76		dB
			±10 MHz offset		83		dB
Image Rejection @ 433 MHz	IMR_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW=4.8 kHz CW interference, BER<0.1%	Before calibration		30		dB
			After calibration		56		dB
Image Rejection @ 868 MHz	IMR_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW=4.8 kHz CW interference, BER<0.1%	Before calibration		26		dB
			After calibration		51		dB
Input 3rd order intercept point @ 433 MHz	$IIP3_{433}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-13		dBm
Input 3rd order intercept point @ 868 MHz	$IIP3_{868}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-12		dBm
Receiver input impedance	Zin	RXP and RXN Differential input impedance	433MHz	150Ω// 0.8pF			
			868MHz	134Ω// 1.0pF			

1.5 Transmitter

Table 5. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific peripheral components are required according to different frequency bands.	-10		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power change in differenttemperature	$P_{OUT-TOP}$	Temperature range: -40 to +85 °C		1		dB
Spurious emissions		P_{OUT} = +13 dBm,433 MHz, F_{RF}<1 GHz			-54	dBm
		1 GHz to 12.75 GHz, including Harmonic			-36	dBm
Harmonic output[1] for F_{RF}= 315 MHz	$H2_{315}$	2^{nd}harmonic, +20 dBm P_{OUT}		-57		dBm
	$H3_{315}$	3^{rd} harmonic,+20 dBm P_{OUT}		-75		dBm
Harmonic output[1] for F_{RF}= 433 MHz	$H2_{433}$	2^{nd} harmonic, +20 dBm P_{OUT}		-56		dBm
	$H3_{433}$	3^{rd} harmonic,+20 dBm P_{OUT}		-71		dBm
Harmonic output[1] for F_{RF}= 868 MHz	$H2_{868}$	2^{nd} harmonic,+20 dBm P_{OUT}		-47		dBm
	$H3_{868}$	3^{rd} harmonic, +20 dBm P_{OUT}		-72		dBm
Harmonic output[1] for F_{RF}= 915 MHz	$H2_{915}$	2^{nd}harmonic,+20 dBm P_{OUT}		-47		dBm
	$H3_{915}$	3^{rd} harmonic,+20 dBm P_{OUT}		-73		dBm
Harmonic output[1]	$H2_{315}$	2^{nd} harmonic, +13 dBm P_{OUT}		-51		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
for F_{RF}= 315 MHz	$H3_{315}$	3rd harmonic,+13 dBm P_{OUT}		-72		dBm
Harmonic output[1] for F_{RF}= 433 MHz	$H2_{433}$	2nd harmonic, +13 dBm P_{OUT}		-44		dBm
	$H3_{433}$	3rd harmonic, +13 dBm P_{OUT}		-58		dBm
Harmonic output[1] for F_{RF}= 868 MHz	$H2_{868}$	2ndharmonic, +13 dBm P_{OUT}		-50		dBm
	$H3_{868}$	3rd harmonic,+13 dBm P_{OUT}		-71		dBm
Harmonic output[1] for F_{RF}= 915 MHz	$H2_{915}$	2nd harmonic, +13 dBm P_{OUT}		-54		dBm
	$H3_{915}$	3rd harmonic,+13 dBm P_{OUT}		-73		dBm

Notes:

[1]. The harmonic levelmainly depends on the quality of matching network. The parameters above are measured based on CMT2310A-EM.

1.6 RF Frequency Synthesizer

Table 6. RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Require different matching networks.	675		960	MHz
			338		640	MHz
			113		320	MHz
Frequency deviation range	F_{DEV_RNG} [1]	675 ~ 960 MHz		600		kHz
		450 ~ 640 MHz		400		kHz
		338 ~ 450 MHz		300		kHz
		225 ~ 320 MHz		200		kHz
		169 ~ 225 MHz		150		kHz
		135 ~ 169 MHz		120		kHz
		113 ~ 135 MHz		100		kHz
Frequency resolution	F_{RES}			60		Hz
Frequency tuning time	t_{TUNE}			60		us
Phase noise @ 433 MHz	PN_{433}	10 kHz Frequency Offset		-101		dBc/Hz
		100 kHz Frequency Offset		-114		dBc/Hz
		1MHz Frequency Offset		-129		dBc/Hz
		10 MHz Frequency Offset		-134		dBc/Hz
Phase noise @ 868 MHz	PN_{868}	10 kHz Frequency Offset		-100		dBc/Hz
		100 kHzFrequency Offset		-109		dBc/Hz
		1MHz Frequency Offset		-126		dBc/Hz
		10 MHz Frequency Offset		-129		dBc/Hz

Notes:

[1]. For 2FSK and 4FSK, F_{DEV} represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.

1.7 Settling Time

Table 7. Settling Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settling time	T_{SLP-RX}	From Sleep to RX		660		us
	T_{SLP-TX}	From Sleep to TX		660		us
	T_{STB-RX}	From Standby to RX		160		us
	T_{STB-TX}	From Standby to TX		160		us
	T_{RFS-RX}	From RFS to RX		16		us
	T_{TFS-RX}	From TFS to TX		16		us
	T_{TX-RX}	From TX to RX (Ramp down requires $2T_{symbol}$ time)		$2T_{symbol}$ +168		us
	T_{RX-TX}	From RX to TX		220		us

Notes:

[1]. T_{SLP-RX} and T_{SLP-TX} mainly depend on crystal oscillating, which is largely related to crystal itself.

1.8 Crystal Oscillator

Table 8. Crystal Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency [1]	F_{XTAL}			32		MHz
Crystal frequency precision [2]	$ppm_{\_XTAL}$		0	20	100	ppm
Load resistance	C_{LOAD_XTAL}			15		pF
Crystal equivalent resistance	Rm_{XTAL}			60		Ω
Crystal startup time [3]	t_{XTAL}			200		us

Notes:

[1]. The CMT2310A can utilize external reference clock to directly drive XIN pin through the coupling capacitor. The peak-to-peak value of external clock signal is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is to a large degree crystal dependent.

1.9 Low-frequency Oscillator

Table 9.Low-frequencyOscillatorSpecifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency accuracy		After calibration		±1		%
Temperature coefficient [2]				-0.02		%/°C
Supply voltage coefficient [3]				+0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Notes:

[1].The low-frequency oscillator is automatically calibrated to the crystal oscillator frequency at the PUP stage.

[2].After calibration,the frequency will drift with temperature.

[3].After calibration,the frequency will drift with the change of the supply voltage.

1.10 Low Battery Detection

Table10. Low Battery Detection Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection accuracy	LBD_{RES}			50		mV

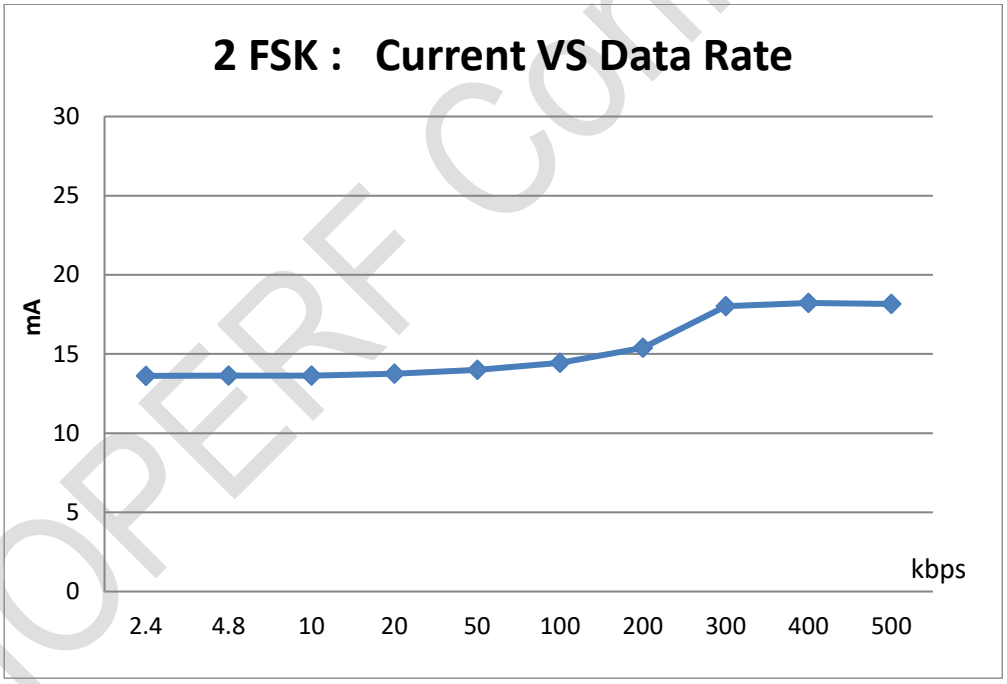
1.11 Digital Interface

Table 11. Digital Interface Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input high level	V_{IH}		Vdd-0.4			V_{DD}
Digital input low level	V_{IL}				0.2	V_{DD}
Digital output high level	V_{OH}	@I_{OH}= -0.5 mA	Vdd-0.4			V
Digital output low level	V_{OL}	@I_{OL}= 0.5 mA			0.4	V
SCLK frequency	F_{SCL}				10	MHz
SCLK high time	T_{CH}		50			ns
SCLK low time	T_{CL}		50			ns
SCLK rising edge time	T_{CR}			10		ns
SCLK falling edge time	T_{CF}			10		ns

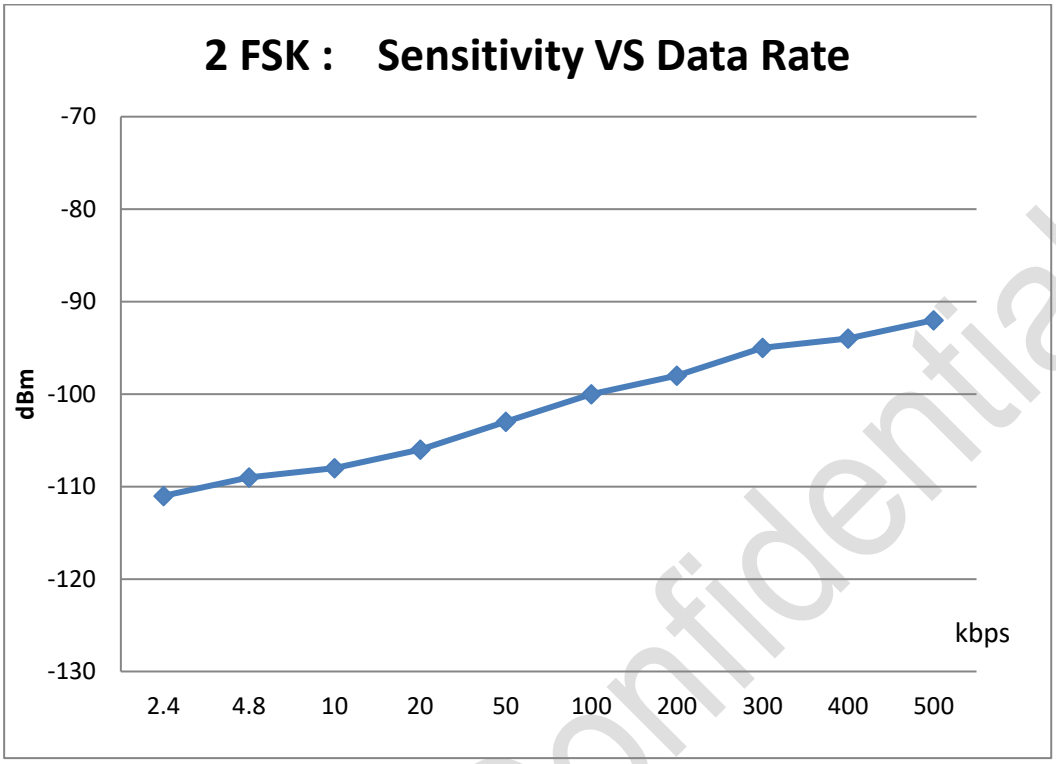
1.12 Typical Parameter Chart

1.12.1 Rx Current Vs. Data rate



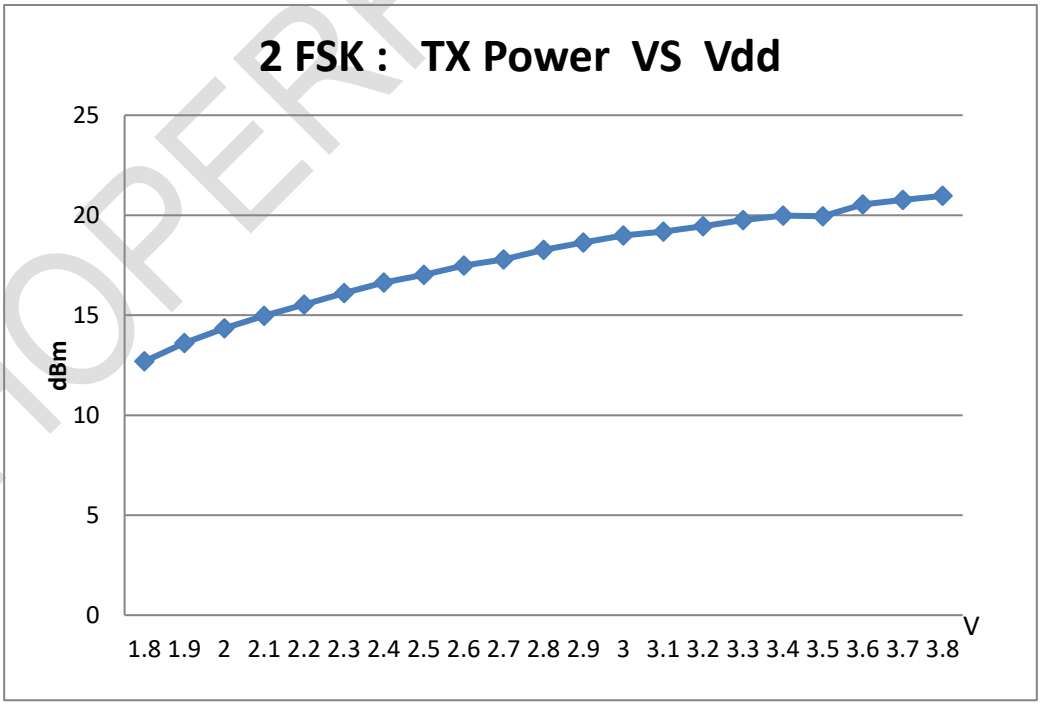
Test condition: Freq = 434 MHz, ppm = 10.

1.12.2 Rx Sensitivity Vs. Data rate



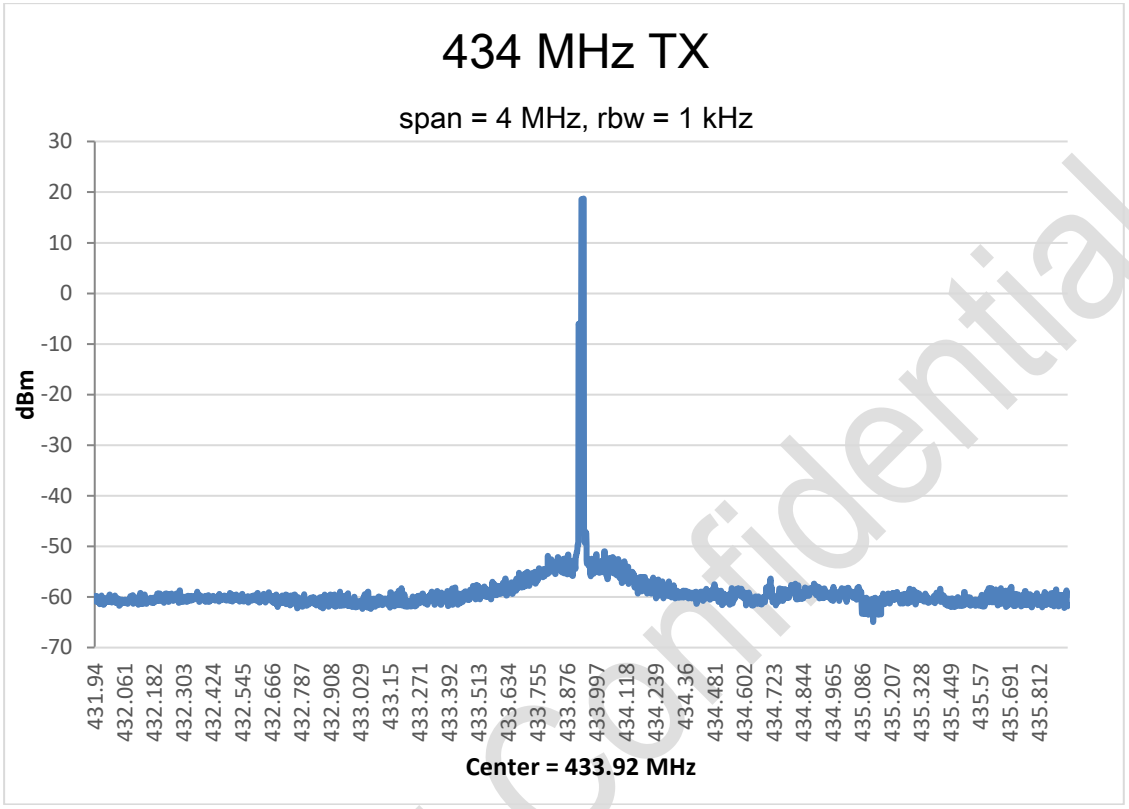
Test condition: Freq = 434 MHz, ppm = 10, BER <=0.1%

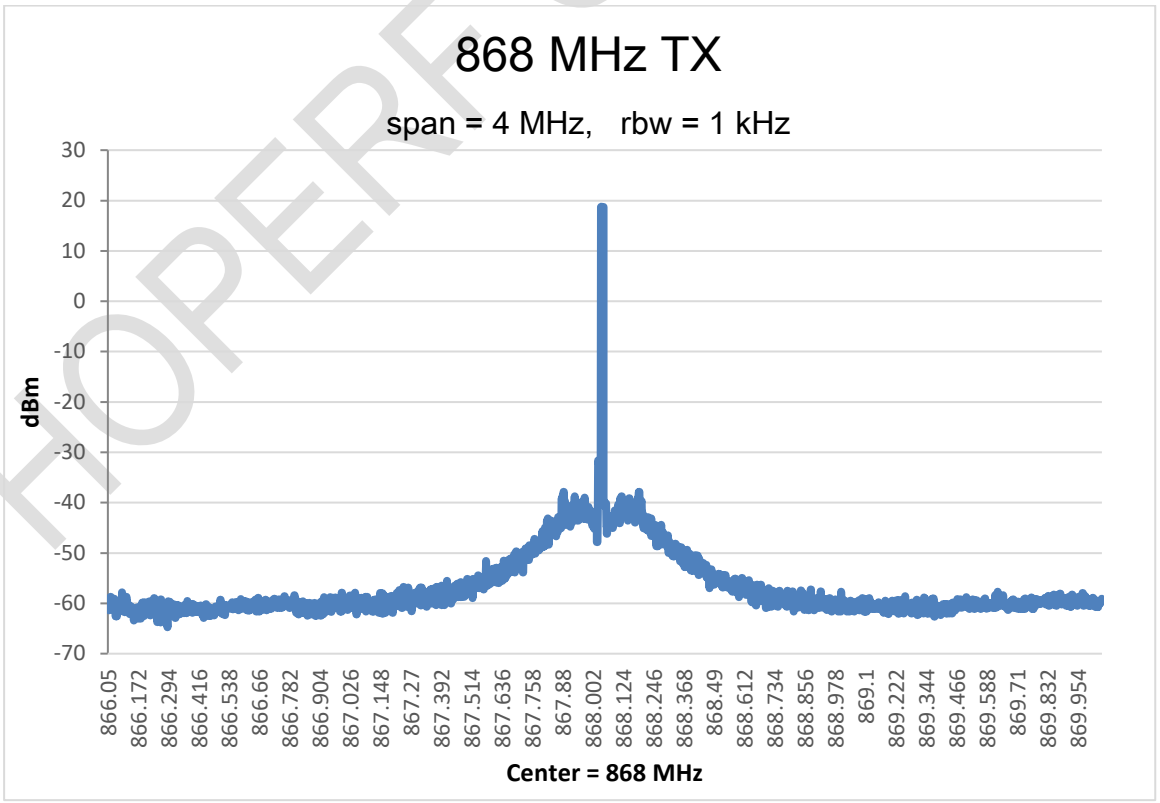
1.12.3 Tx Power Vs. Supply Power Voltage



Test condition: Freq = 434 MHz, 20 dBm matching network, Tx power with 3.3 V and 20 dBm

1.12.4 Tx Phase Noise





2 Pin Descriptions

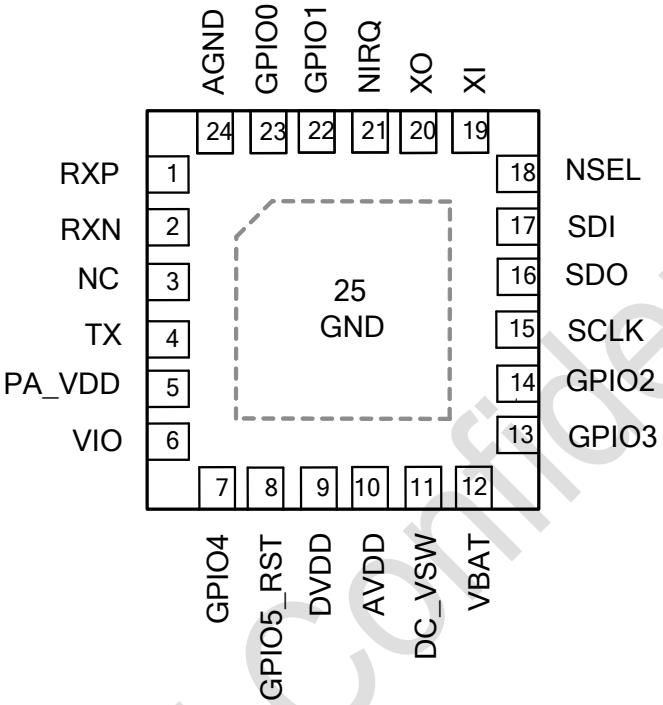


Figure 1. CMT2310A Pin Arrangement

Table 12. CMT2310A Pin Description

Pin #	Pin Name	I/O	Description
1	RXP	I	RF signal positive input
2	RXN	I	RF signal negative input
3	NC	O	Floating, not connected
4	TX	O	Tx output
5	PA_VDD	IO	PA VDD
6	VIO	IO	IO VDD
7	GPIO4	IO	Configurable, see *Table 17 CMT2310A GPIO* for more details.
8	GPIO5_RST	IO	Configurable, see *Table 17 CMT2310A GPIO* for more details.
9	DVDD	I	Digital VDD
10	AVDD	I	Analog VDD
11	DC_VSW	I	DCDC
12	VBAT	I	Analog VDD
13	GPIO3	IO	Configurable, see *Table 18 CMT2310A GPIO* for more details.
14	GPIO2	IO	Configurable, see *Table 18 CMT2310A GPIO* for more details.
15	SCLK	I	SPI clock.
16	SDO	O	SPI data output.
17	SDI	I	SPI data input.
18	CSB	I	Chip select bar

19	XI	I	32M Crystal circuit input.
20	XO	O	32M Crystal circuit output.
21	NIRQ	I	Configurable, see *Table 17 CMT2310A GPIO* for more details.
22	GPIO1	IO	Configurable, see *Table 17 CMT2310A GPIO* for more details.
23	GPIO0	IO	Configurable, see *Table 17 CMT2310A GPIO* for more details.
24	AGND	I	Analog GND.
25	GND	I	GND

3 Typical Application Schematic

3.1 Direct Tie Schematic Diagram

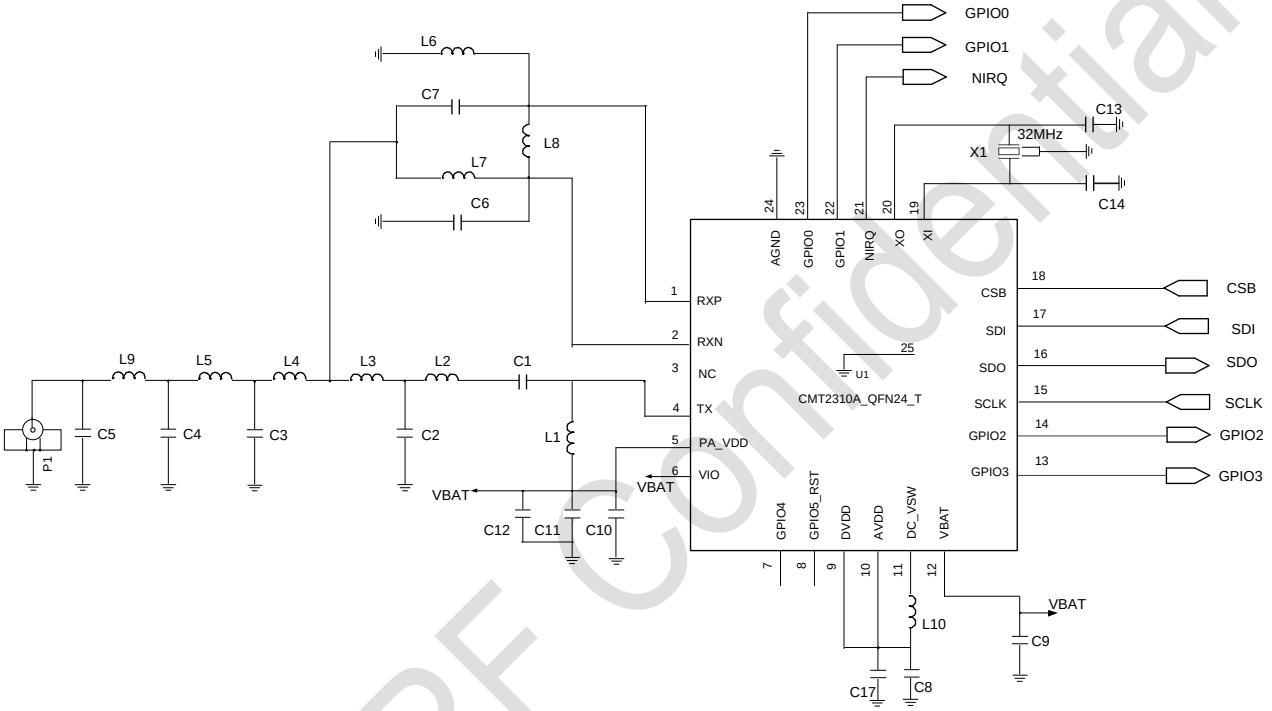


Figure 2. Direct Tie Application Schematic Diagram (DCDC enabled)

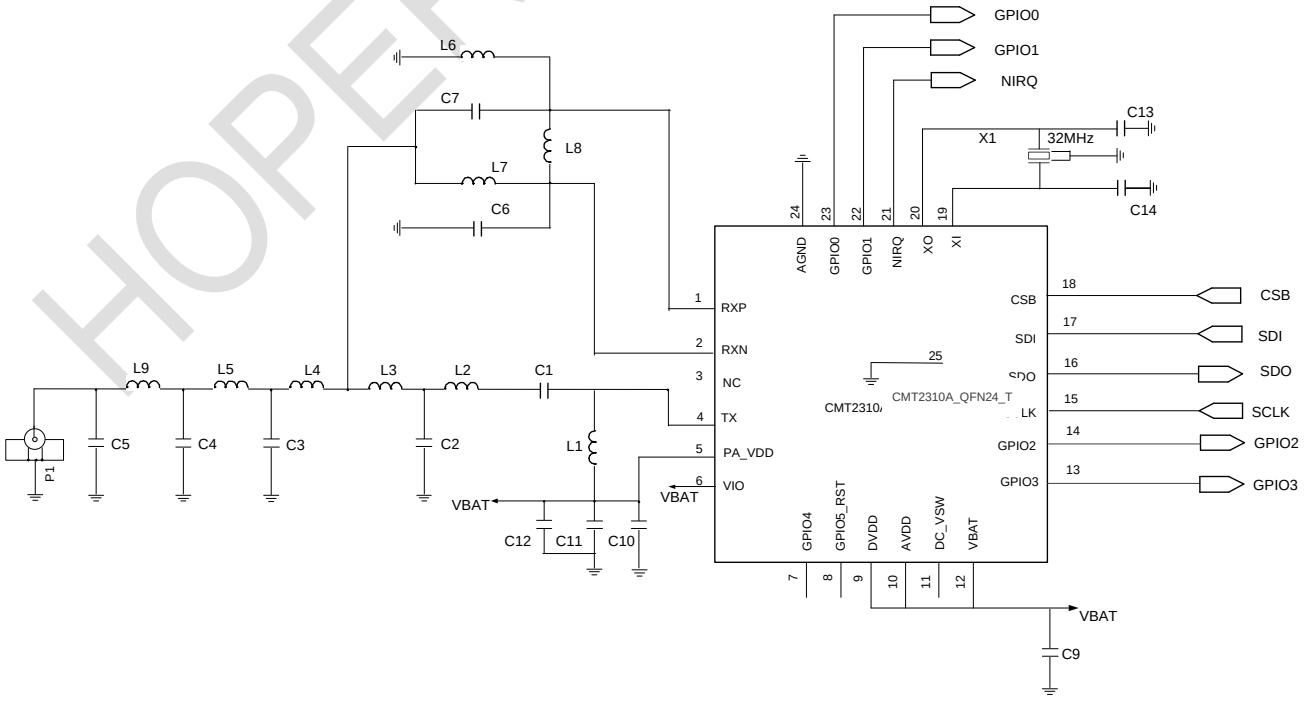


Figure3. Direct Tie Application Schematic Diagram (DCDC disabled)

Table 3-1. 20 dBm Direct Tie Application BOM

No.	Descriptions	Component Values				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	22	12	12	12	pF	
C2	±5%, 0402 NP0, 50 V	6.8	5.6	3.3	3.3	pF	
C3	±5%, 0402 NP0, 50 V	8.2	6.2	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	8.2	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
C17	±5%, 0402 NP0, 50 V	100				nF	
L1	±5%, 0603 Chip Ceramic Inductor	220	180	100	100	nH	Sunlord
L2	±5%, 0603 Chip Ceramic Inductor	68	47	15	12	nH	Sunlord
L3	±5%, 0603 Chip Ceramic Inductor	56	39	15	12	nH	Sunlord
L4	±5%, 0603 Chip Ceramic Inductor	33	33	8.2	6.2	nH	Sunlord
L5	±5%, 0603 Chip Ceramic Inductor	47	33	8.2	6.2	nH	Sunlord
L6	±5%, 0603 Chip Ceramic Inductor	47	33	15	12	nH	Sunlord
L7	±5%, 0603 Chip Ceramic Inductor	47	33	15	12	nH	Sunlord
L8	±5%, 0603 Chip Ceramic Inductor	220	68	33	33	nH	Sunlord
L9	±5%, 0603 Chip Ceramic Inductor	33	NC	NC	NC	nH	Sunlord
L10	MPH252012C100MT, 10UH ±20%, Package 2520, DC Resistance 0.5 Ω , Saturation Current 0.5A	10				uH	Sunlord
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2310A RF receiver and transmitter					-	CMOSTEK

Table 3-2. 13 dBm Direct Tie Application BOM

No.	Descriptions	Component Values				Unit	Supplier
		315 MHz +13 dBm	433 MHz +13 dBm	868 MHz +13 dBm	915 MHz +13 dBm		
C1	±5%, 0402 NP0, 50 V	8.2	18	15	15	pF	
C2	±5%, 0402 NP0, 50 V	3.9	5.6	3.9	4.3	pF	
C3	±5%, 0402 NP0, 50 V	9.1	6.8	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	9.1	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
C17	±5%, 0402 NP0, 50 V	100				nF	
L1	±5%, 0603Chip Ceramic Inductor	220	180	100	100	nH	Sunlord
L2	±5%, 0603Chip Ceramic Inductor	56	56	15	12	nH	Sunlord
L3	±5%, 0603Chip Ceramic Inductor	10	47	15	12	nH	Sunlord
L4	±5%, 0603Chip Ceramic Inductor	33	15	8.2	8.2	nH	Sunlord
L5	±5%, 0603Chip Ceramic Inductor	56	15	8.2	8.2	nH	Sunlord
L6	±5%, 0603Chip Ceramic Inductor	47	33	15	12	nH	Sunlord
L7	±5%, 0603Chip Ceramic Inductor	47	33	15	12	nH	Sunlord
L8	±5%, 0603Chip Ceramic Inductor	220	68	33	33	nH	Sunlord
L9	±5%, 0603Chip Ceramic Inductor	33	NC	NC	NC	nH	Sunlord
L10	MPH252012C100MT, 10UH ±20%, Package 2520, DC Resistance 0.5Ω, Saturation Current 0.5A	10				uH	Sunlord
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2310A RF receiver and transmitter					-	CMOSTEK

4 Function Description

The CMT2310A is a high integrated mixed-signal transceiver, which employs a 32 MHz crystal to provide PLL reference frequency and digital clock with supporting of OOK, 2-(G)FSK, 4(G)FSK modulation/demodulation as well as Direct and Packet Data processing modes.

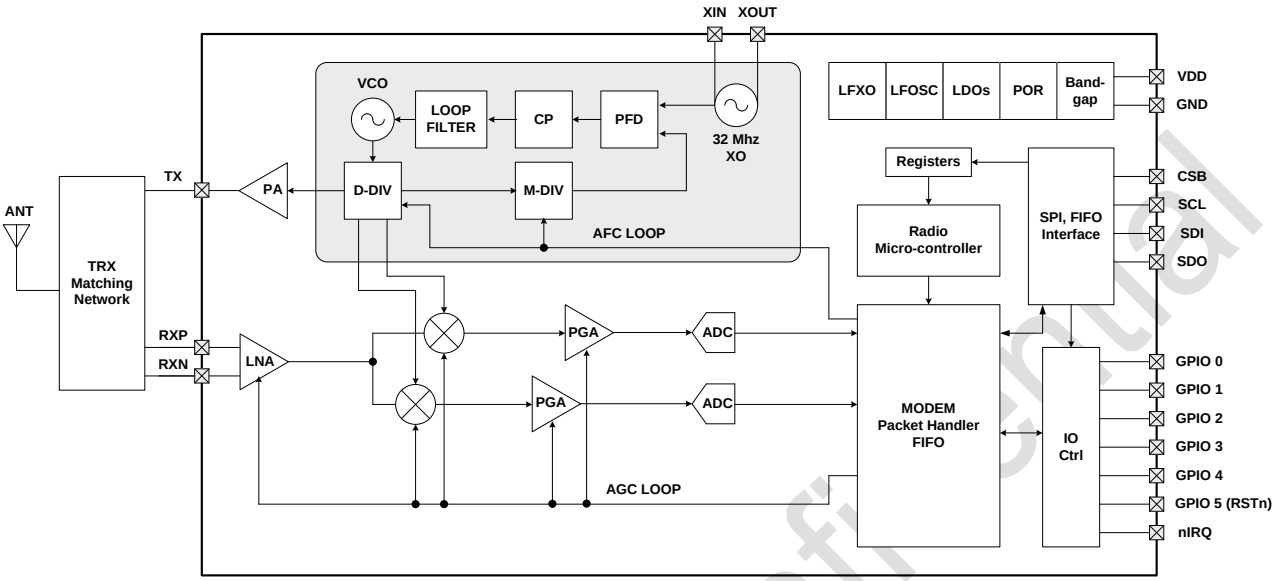


Figure 2. Functional Block Diagram

In receiver part, the chip applies LNA+MXR+PGA+ADC+PLL low-IF architecture to achieve the Sub-GHz wireless receiving function. In transmitter part, it applies PLL+PA architecture to achieve the Sub-1 GHz wireless transmitting function. The chip can achieve high-performance RF transmission and receiving with no need of extra RF switch components,

In the receiver system, the analog circuit mixes the RF signal to IF and converts the signal from analog to digital through ADC module, then outputs the two signal paths I/Q tothe digital circuit for digital demodulation.The digital circuit is responsible formixing the IF signal to zero-frequency (baseband) and performing a series of filtering and decision processing, meanwhile it applies AFC and AGCto control the analog circuit dynamically, and finally the original signal is demodulated. After demodulation, the signal is sent to the decoder for decoding and then filled into FIFO, or output to GPIO directly.

In the transmitter system, the digital circuit encodes and packets the data then sends it to the modulator (or send data directly to modulator without encoding). Then modulator will directly control the PLL and PA to have 2(G)FSK, 4(G)FSK or OOK based modulation then transmit out the data.

The chip integrates a mini micro-controller (supporting supplier internal programming only), which controls and schedules various functions and operations like auto-ACK, auto-frequency-hopping, DUTY-CYCLE based low-power Tx and Rx, CSMA function, etc.

The chip provides SPI communication port. The external MCU can access registers to have various function configures, to control the chip or access FIFO.

4.1 Transmitter

Thetransmitter of CMT2310Ais based on direct frequency synthesis technology. Its carrier is generated by a low-noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via the register, with configurable value ranging from -10 dBm to +20 dBm by a step of 1dB.

In OOK mode, when PA switches on and off quickly according to data transmitted, it will easily produce spectral spurs and glitches near the target carrier. Through the PA Ramping mechanism, it can help to minimize the spurs and glitches. In FSK mode, the transmitter supports to have Gaussian filtering on signals before transmission, namely GFSK, thus to make the transmitting spectrum more concentrated.

Users can design a PA matching network based on specific application requirements to optimize the transmission efficiency at the required output power. Typical application schematics and required BOMs are detailed in *Section 3 Typical Application Schematic*.

The transmitter can work in direct mode and packet mode respectively. In direct mode, data is sent to the chip directly through pin of the chip then transmitted directly. In packet mode, data can be pre-loaded into the FIFO in STBY status and then transmitted along with other packet elements. In 4FSK mode, it only supports data transmitting from FIFO.

4.2 Receiver

An ultra-low-power, high-performance low-IF OOK/ FSK receiver is built in the CMT2310A. Its processing steps are as follows: 1) the RF signal sensed by the antenna is amplified by the low-noise amplifier; 2) the signal is down-converted to the intermediate frequency by the quadrature mixer; 3) the signal is further amplified by the programmable amplifier; 4) The signal is sent to the digital domain through A/D convertor for digital demodulation processing. During power on reset (POR), each analog module is calibrated to the internal reference voltage. This allows the chip to keep its best performance at different temperatures and voltages. Baseband filtering and demodulation is accomplished by the digital demodulator. The AGC loop adjusts the system gain to optimize the performance parameters such as system linearity, selectivity and sensitivity.

Leveraging CMOSTEK's low-power design technology, the receiver in always-on mode consumesonly a very low power. The periodic operating mode and wake-up function can furtherreduce the average power consumption of the system to satisfy applications with strict power consumption requirements.

Similar to the transmitter, the CMT2310A receiver can operate in direct mode and packet mode as well. In direct mode, the demodulator output data can be directly output through the DOUT pin of the chip. DOUTcan be assigned to GPIO by configuration. In packet mode, the demodulator data output is sent to the data packet handler, get decoded then is filled into the FIFO, then MCU can read the FIFO through SPI interface.

4.3 Additional Functions

4.3.1 Power-On Reset (POR)

The power-on reset circuit detects the change of the VDD power supply and generate reset signal to reset the entire CMT2310A system. After the POR,the MCU must go through initialization process and re-configure the CMT2310A.There are two situations that will lead to the generation of POR.

The first situation is a very short and sudden decrease of VDD. The corresponding POR triggering condition is that VDD dramatically decreases by 0.9V+/- 20% (namely 0.72V – 1.08V) within less than 2 us. To be noticed, it detects a decreasing amplitude of the VDD but not the absolute value of VDD as shown in the figure below.

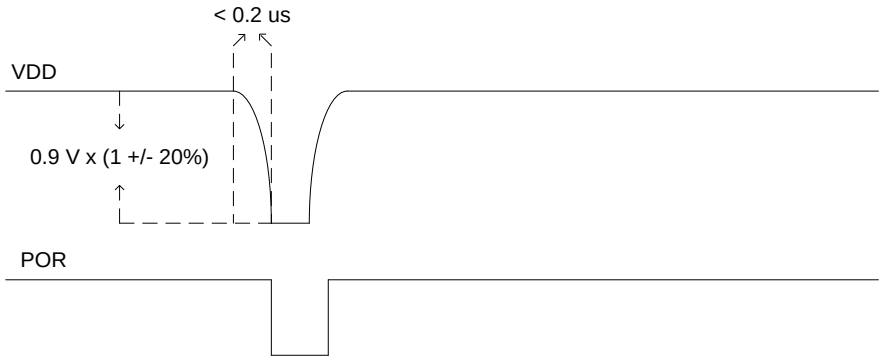


Figure 3. Sudden Decrease of VDD Leading to Generation of POR

The second situation is a slow decrease of the VDD. The corresponding POR triggering condition is that VDD decreases to 1.45V +/- 20% (namely 1.16 ~ 1.74V) within a time more than or equal to 2 us. To be noticed, it detects an absolute value of VDD but not the decreased amplitude as shown in the figure below.

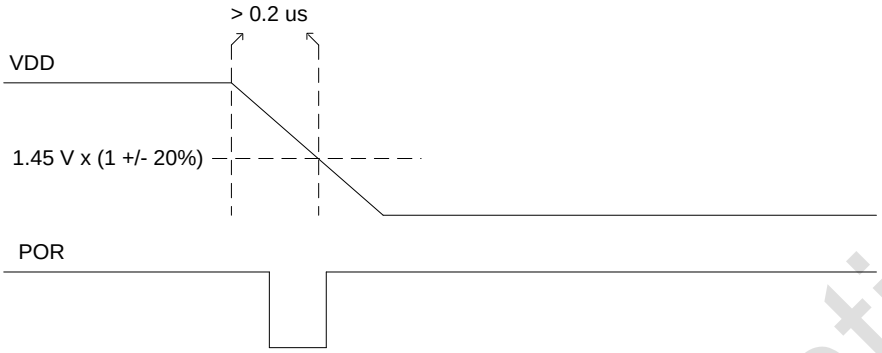


Figure 4. Slow Decrease of VDD Leading to Generation of POR

4.3.2 Crystal Oscillator

The crystal oscillator provides the reference clock for PLL as well as the system clock for digital module. The value of load capacitance depends on the C_L parameter according crystal specification. The total load capacitance between XI and XO should be equal to C_L, in order to make the crystal accurately oscillate at 32 MHz.

$$\mathbf{C_L = \frac{C_{on_{chip}} + C_{off\_chip} + C_{par}}{2}}$$

$C_{on\ chip}$ is the on-chip load capacitor connected at both ends of the crystal with a adjustable value range of 23 - 29 pF by a step of about 190 fF. C_{off} c_{hip} is the external load capacitor connected at both ends of the crystal to ground, which is optional, i.e. it's up to user whether to apply it. Cpar is the parasitic capacitor connected at both ends of the crystal to ground with a value of about 2 ~6pF. A crystal oscillatorof 15 pF is recommended to collaborate with CMT2310A. Besides, the less the ppm value of the crystal, the better the performance of the receiver.

4.3.3 Temperature Compensated Crystal Oscillator (TCXO)

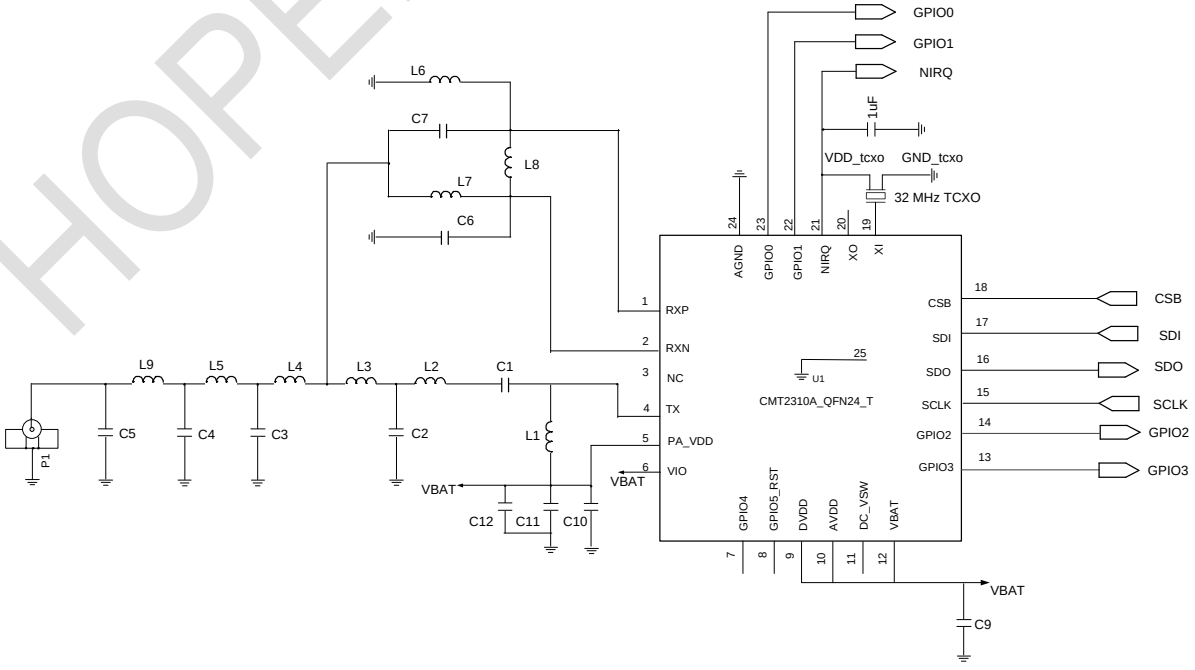


Figure 5. Application Schematic Diagram with TCXO

The CMT2310A allows users to apply external clock modules such as temperature compensated crystal oscillator (TCXO). The application schematic diagram is shown in the above figure. The VDD pin of TCXO is powered by connecting the NIRQ pin of the CMT2310A. By setting NIRQ_SEL as 4, setting Output Drive Capability as 4 mA on RFPDK, and adding a filter capacitor of 1 uF, users can gain sound application effect. The 32 MHz clock of the TCXO is connected directly tothe XI pin. The TCXO is disabled by the system in the IDLE and SLEEP states, and it's enabled in the other states.

The recommended peak-to-peak value range of this clock signal is 300 ~ 700 mV. Users can add both a capacitor to ground and a DC-blocking capacitor connecting the XI pin. Through tuning the proportion of these two capacitors, users can adjust the amplitude amount of the input clock. Applying TCXO will approximately cause a increase of the overall current by 1.5 ~2.0 mA. The more precise clock (<2ppm) enables the CMT2310A to attain higher sensitivity and better capability against out-of-band interference while operating in a narrower receiving bandwidth.

4.3.4 Sleep Timer

The 2310A integrates a sleep timer driven by 32 kHz low-power oscillator (LPOSC) or external 32.768 kHz low-frequency crystal (LFXO).When this function is enabled, the timer wakes up the chip from sleep periodically.When the chip operates in periodic mode, the sleep time can be configured from 62.5 us to 8585740.288 s. As the low-power oscillator frequency will change with the temperature and voltage drift, thus it will be automatically calibrated during power-on and will be periodically calibrated since then. These calibrations will keep the frequency tolerance of the oscillator within + 1%. The precision of the external low-frequency crystal depends on specific crystal characteristics.

4.3.5 Low Battery Detection

The chip supports low battery detection function. When the chip istuned to a certain frequency, the detection will be performed once. Frequency tuning happens when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_VALUE register.

4.3.6 Received Signal Strength Indicator (RSSI)

RSSI is used to evaluate the signal strengthinside the channel with a detection range of -127 to 20 dBm. On RFPDK tool, users can configure the parameter RSSI Detect Mode to choose whether output real-time RSSI value or latch the RSSI values in different data packet processing states.

CMT2310A allows users to configure RSSI detection threshold through RFPDK parameter RSSI Compare TH. This threshold value will be compared with the RSSI detection value. If the RSSI detection value is larger than the threshold it outputs logic 1, otherwise outputs logic 0. The comparison result output can be used as a source of the RSSIVLD interrupt, or used to support internal super-low power (SLP) mode operating.

4.3.7 Phase Jump Detector (PJD)

PJD is Phase Jump Detector.When the chip isin 2-FSK demodulation, it can automatically observethe phase jump characteristics of the received signal to determine whether it isa noise or useful signal.

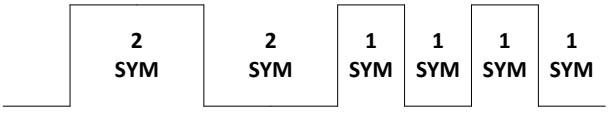


Figure 6. Received Signal Jump Diagram

The PJD mechanism regards input signal switching from 0 to 1 or from 1 to 0 as a phase jump. Users can configure PJD_WIN_SEL<1:0> to determine the number of detected jumpsfor the PJD to identify a wanted signal.As shown in the figure above, in total 8 symbols received, the phase jump appears only 6 times. Therefore, the number of jumps is not equal to the number of symbols received. Only in the preamble receiving period they are equal. In general, the more jumps are used to identify the signal, the more reliable the result; the less jumps are used, the faster the result is obtained. If the RX time is set to a relatively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, namely the chip will not mistakenly

treat an incoming noise as a wanted signal, and will not treat a wanted signal as noise either.

The signal phase jump is used for detecting whether the signal has the expected data rate. Meanwhile, the PJD will also automatically detect the signal deviation to see if it meets the valid signal value criteria, aswell as to see if the SNR is over 7 dB. Then by considering data rate, deviation, and SNR detecting results, the PJD makes judgment. If a signalis judged as a reliable signal, it outputs logic 1, otherwise outputs logic 0.The output can be used as a source of the RSSI VLD interrupt, or output internally to support the super-low power (SLP) mode operating.In direct data mode, when setting the DOUT_MUTE register bit to 1, the PJD mechanism can be utilized to fulfill the mute function of FSK demodulation output.

The PJD technique is similar to traditional carrier sense (CS) technique but more reliable.By combining PJD technique with RSSI detection, users can accurately identify the idle/busy statusof the current channel.

4.3.8 Automatic Frequency Control (AFC)

The AFC mechanism allows the receiver to minimize the frequency error between the TX and RX in a very short time once a wanted signal comes in. This helps the receiver to maintain an optimized sensitivity performance. CMT2310A provides an competitive AFC technology in the industry, that is, within the same bandwidth, the CMT2310A can identify larger frequency error, and remove the error in a much shorter time (8-10 symbols).

Normally the frequency variance between the TX and RX is caused by thefrequency variance of the crystal oscillators used in the both sides. The CMT2310A allows users to fill in the crystal tolerance value (in PPM) of TX and RX on RFPDK. Based on the crystal tolerance value, the RFPDK configures the AFC detecting range meanwhile trying to minimize the bandwidth used by the receiver. With the excellent performance of the AFC, the product offers a favorable solution to the crystal aging problem which will lead to more frequency variance as time goes on.Therefore, comparing with other similar transceiver chips in the industry, the CMT2310A can settle down more severe crystal aging problems and extend product life time effectively.

4.3.9 Clock Data Recovery (CDR)

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate while receiving the data,not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data.So CDR's task is simple yet very important. If it has error between the recovered clock frequency and the actual symbol rate, it will cause data acquisition error, code error and decoding error during data receiving.

The CMT2310A provides three types of CDR systems as follows.

1. **COUNTING system** - The system is designed according to the case of relatively accurate symbol rate.If the symbol rate is100% aligned, the unlimited length of 0 can be received continuously without error.

2. **TRACING system** - The system is designed according to the case of larger symbol rate error.It has tracking function, that is,it can automatically detect the Tx transmission symbol rate,and adjust the local symbol rate of RX quickly at the same time,so as to minimize the error between them.The system can withstand up to about 15.6% symbol rate error, an excellent level among similar products in the industry.

3. **MANCHESTER system** -This system evolves from the COUNTING system with the same basic features.The only difference is that the system is specially designed for Manchester code. It supports special processing to handle unexpected changes of TX symbol rate.

4.3.10 Fast Frequency Hopping

The mechanism of fast frequency hopping is that, based on the frequency configured on the RFPDFK like 433.92 MHz, the MCU can quickly switch to another frequency channel by simply changing 1 or 2 registers in application procedures. This can much more simplify the operation of frequently changing the RX orTX frequency in multi-channel applications.

$$\mathbf{FREQ} = \mathbf{Base\ Freq} + \mathbf{2.5\ kHz} \times \mathbf{FH\_OFFSET} < \mathbf{7:0} > \times \mathbf{FH\_CHANNEL} < \mathbf{7:0} >$$

In general, users can configure FH_OFFSET<7:0> during the chip initialization process, and then in the applicationusers can switch the channel by changing FH_CHANNEL<7:0>.

5 Chip Operation

5.1 SPI Interface

5.1.1 Read/Write Register

The chip communicates with the outside through the 4-wire SPI interface, which is 4-wire by default and can be configured as 3-wire. The CSB is the active-low chip selection signal for accessing registers. The SCLK is the serial clock with a highest speed of 10 MHz. Either the chip itself or the external MCU sends out data at the falling edge of SCLK and captures the data at the rising edge of SCLK. The SDI is for data input and SDO for data output. In 3-wire mode, SDI is used as input and output at the same time and SDO is idle. Both address and data are transferred starting from the MSB.

During register accessing, CSB should be pulled low and R/W bit is sent first followed by a 7-bit register address. After the external MCU pulls CSB low, it must wait for at least half a SCLK cycle then sends the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle then pulls CSB high.

It should be noted that, for 4-wire based register write as shown in the figure below, during SDI input writing data, meanwhile SDO is outputting the current value of the register (old register read data), MCU can choose whether to read this register value depending on specific requirements.

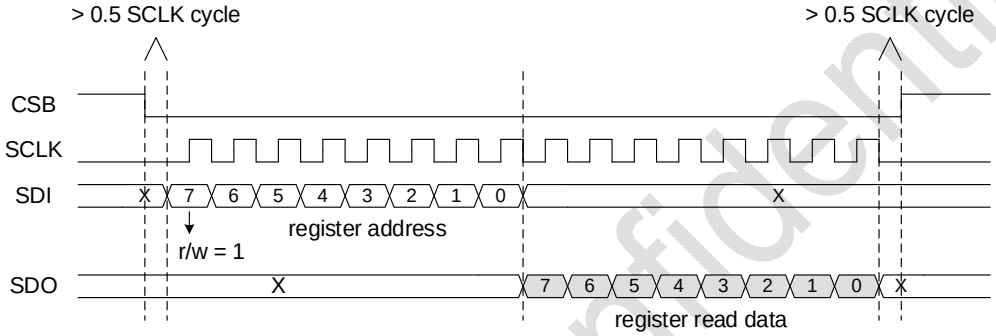


Figure 7. SPI (4-wire) Read Register Timing

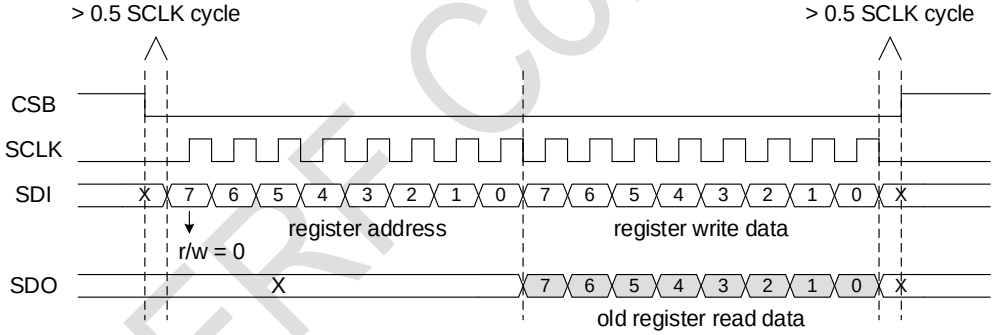


Figure 8. SPI (4-wire) Write Register Timing

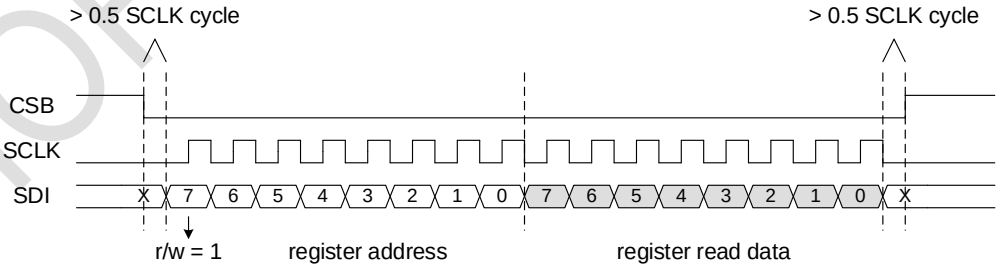


Figure 9. SPI (3-wire) Read Register Timing

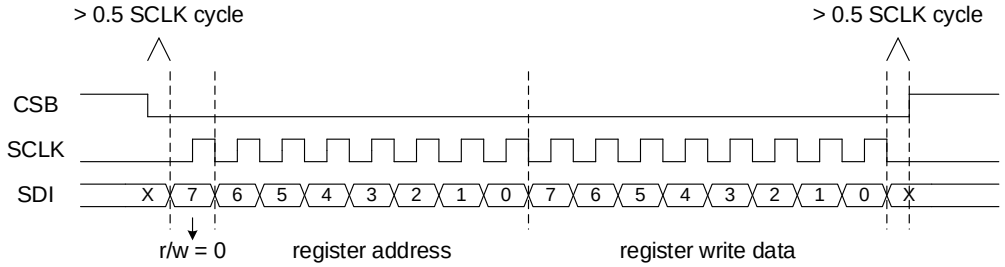


Figure 10. SPI (3-wire) Write Register Timing

For 3-wire based register reading operation, both MCU and CMT2310A will have to switchthe direction of their IO (SDIO) between the address bit 0 and the data bit 7, that is, the CMT2310A should switch from input to output, while the MCU from output to input. As shown in the above figure, please notice the dot line in the middle, here strongly suggest that the MCU switches the IO to input mode before sending out the falling edge of the SCLK; as for CMT2310A, it should switch the IO to output mode after it has gotten the falling edge of the SCLK. This can avoid the possible electrical conflict caused by both of them setting SDIO as output. For MCU, this kind of problems may cause reset or other abnormal behaviors.

5.1.2 Read/Write Register in Batch Mode (BURST)

Besides the single-byte based register read/write stated above, SPI can also support Burst based register read/write. The BURST read/write operation is triggered by writing to the address BRW_PORT of Page 0x7B. When the r/w bit is 0, the register will be written, while as it was 1, the register will be read.

The BURST read/write can also be performed via 3-wire SPI. When 3-wire is used, outputting read data and inputting write data are both performed on the SDI pin. When using 4-wire, write data is input from SDI, and read data is output from SDO. The operation flow of the BURST read/ write is that: accessing the FIFO operation port at the address 0x7B first (the write/read bit inside determines whether it is a read or write operation), then followed by a stage of data reading/writing all along until users determine to complete the operation.

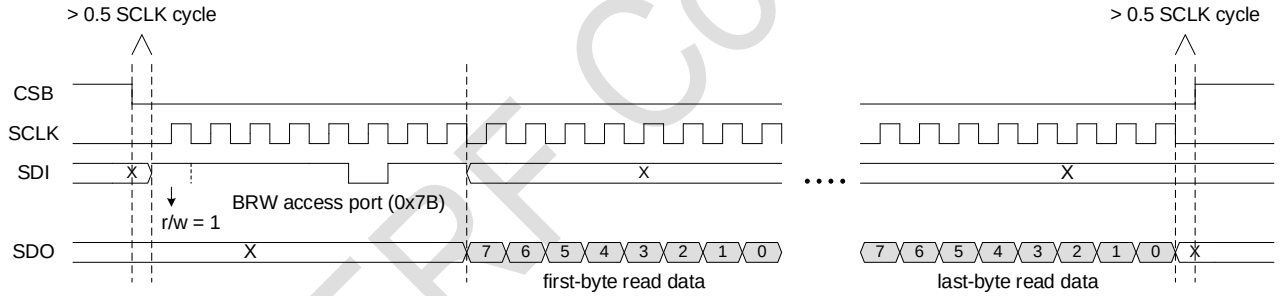


Figure 11. SPI (4-wire) BURST Read Register Timing

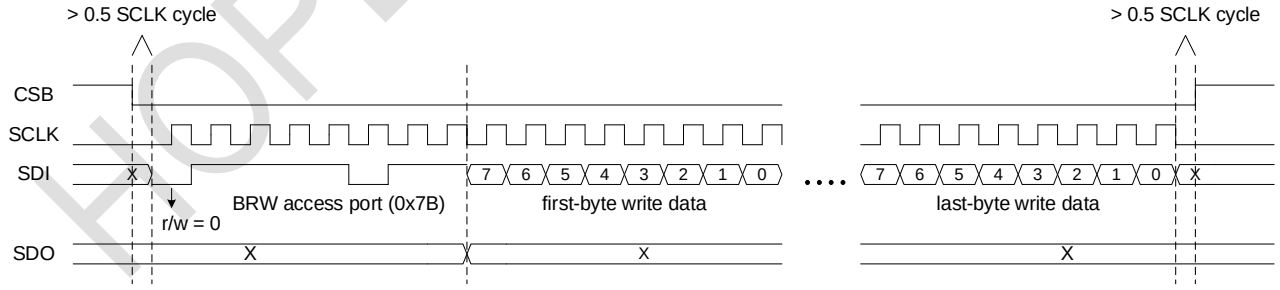


Figure 12. SPI (4-wire) BURST Write Register Timing

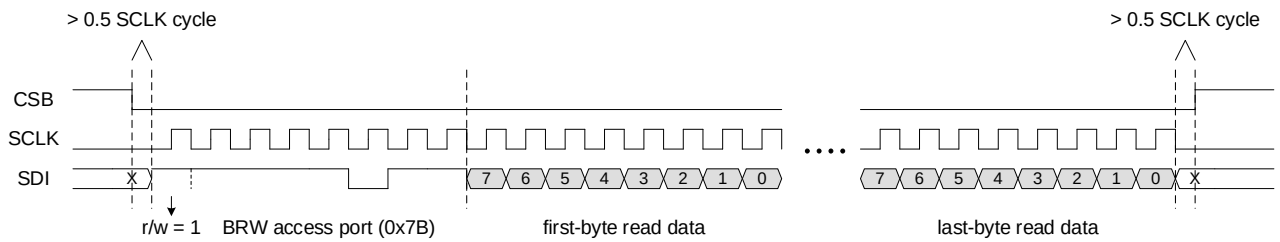


Figure 13. SPI (3-wire) BURST Read Register Timing

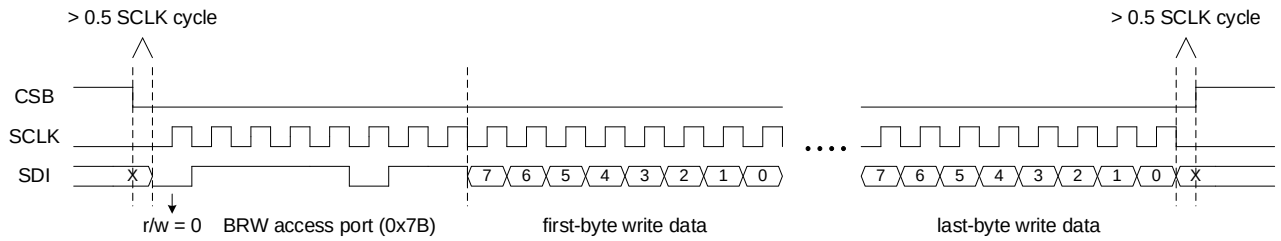


Figure 14. SPI (3-wire) BURST Write Register Timing

It should be noted that the BURST read/write does not support an operation crossing pages, that is, a BURST can only be accomplished within a page. The address ranges supporting the BURST read/write within each page are listed in the table below.

PAGE	Start Address	End Address	The number of addresses	Description
0	0x28	0x77	80	Configuration registers in Page0
1	0x00	0x6F	112	Configuration registers in Page1
2	0x00	0x3F	64	Frequency hopping table in Page2

Users can select any starting address within the address range of each Page for continuous BURST read and write operations of N addresses. The end address cannot exceed the address range according to the value of N. The common way of BURST reading and writing is to allow users to carry out quick one-time configuration before powering on. The configuration register content comes from RFPDK tool, and the content of frequency hopping table is designed by users themselves.

5.2 FIFO

The CMT2310A provides two separated 128-byte FIFO by default. They are used for RX and TX respectively. RX FIFO is used to store received data in Rx mode while TX FIFO is used to store data to be transmitted in Tx mode. Users can also set FIFO_MARGE_EN to 1 to merge the two separated FIFO into one 256-byte FIFO, which is used both in TX and RX mode. By configuring the FIFO_RX_TX_SEL, it can indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the TX FIFO to prepare for the next transmission meanwhile the RX FIFO is being filled in, thus to save system operating time.

The FIFO can be accessed via the SPI interface. Users can clear the FIFO by setting FIFO_CLR_TXor FIFO_CLR_RX to 1. Also, users can re-send the old datain the TX FIFO by setting FIFO_RESTORE to 1, with no need to re-fillthe data.

Users can control whether FIFO still store data in sleep mode by configuring PD_FIFO, that is, PD_FIFO = 0 stands for FIFO storing data in sleep mode, yet with consuming about 200 nA leakage current.

5.2.1 FIFO Read Operation

To access FIFO, the MCU should first configure a few registers to setup the FIFO read/write mode, as well as some other operating modes. As shown in the figure below, it is the read and write timing in determined operating mode. FIFO operation is triggered by writing into address 0x7A in Page 0, it will trigger write operation when r/w bit is 0 and trigger read operation when r/w bit is 1.

FIFO read/writer operations can also be done through 3-wire SPI. In 3-wire SPI case, read data output and write data input are all fulfilled on SDI pin, while in 4-wire SPI case write data is input on SDI, and read data is output on SDO. The procedure of FIFO is: access address of 0x7A first, namely the FIFO operation port with the r/w bit determining whether it is read or writer operation; then continue reading or writing data, and when to finish is determined by users.

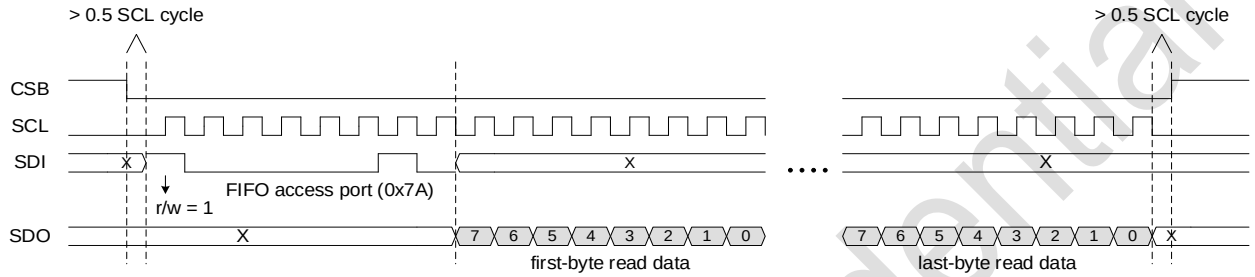


Figure 15. SPI (4-wire) Read FIFO Timing

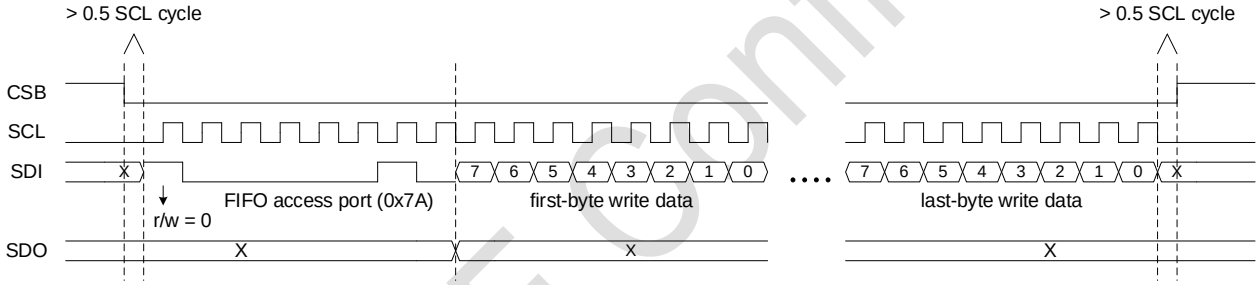


Figure 16. SPI (4-wire) Write FIFO Timing

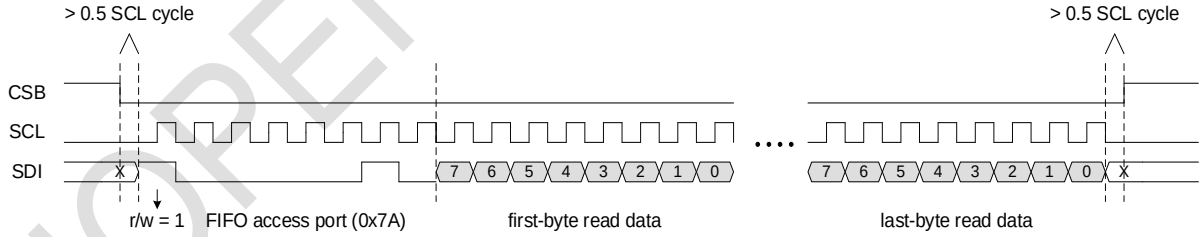


Figure 17. SPI (3-wire) Read FIFO Timing

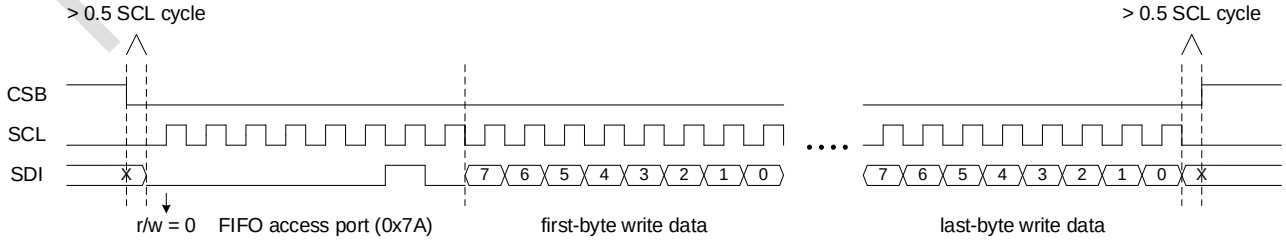


Figure 18. SPI (3-wire) Write FIFO Timing

5.2.2 FIFO Associated Interrupt

CMT2310A provides comprehensive interrupt sources associated with the FIFO. The interrupt timing of Tx and Rx FIFO is shown in the figures below.

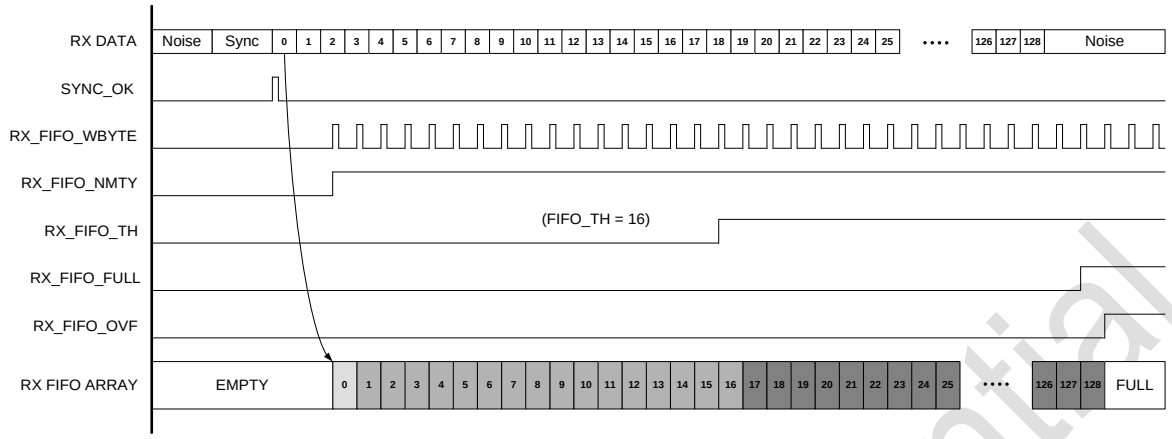


Figure 19. CMT2310A RX FIFO Interrupt Timing

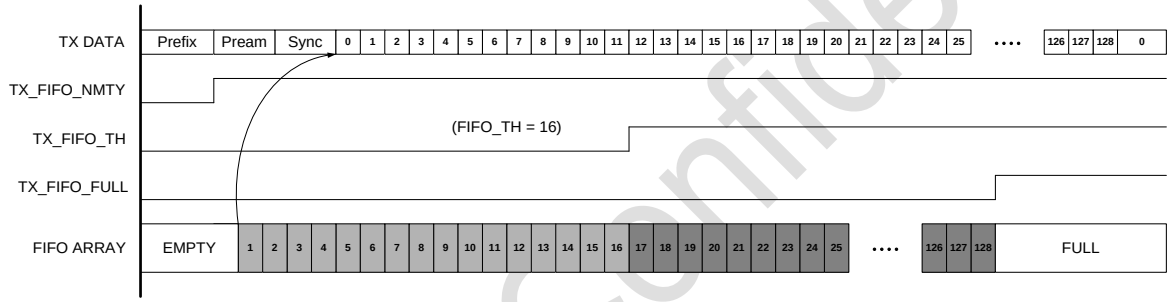


Figure 20. CMT2310A TX FIFO Interrupt Timing

5.3 Operation State, Timing and Power Consumption

5.3.1 Startup Timing

When the chip VDD is powered up, it usually needs to wait about 1ms, then POR will release and chip stays in IDLE state with no operations. When users send power_up command, the chip begins power up procedure to have calibration of all modules. The chip stays in SLEEP mode after calibration done. Any time when reset occurs (including POR, hardware reset and software reset), the chip will return to IDLE state then wait for users to send power_up command.

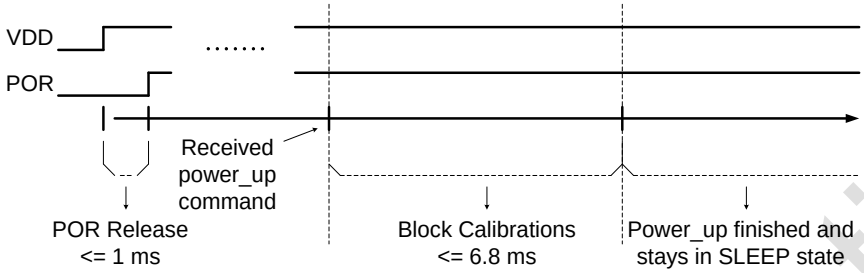


Figure 21. Power-on Timing

5.3.2 Operation State

The CMT2310A supports 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown in the figure below.

Table 13. CMT2310A State and Corresponding Active Module

State	Binary code	Switch ommand	Active Modules	Optional Moduels
IDLE	0x00	soft_rst	SPI, POR	None
SLEEP	0x81	go_sleep	SPI, POR	LFOSC, FIFO, Sleep Timer
READY	0x82	go_ready	SPI, POR, XTAL, FIFO	None
RFS	0x84	go_rfs	SPI, POR, XTAL, PLL, FIFO	None
TFS	0x88	go_tfs	SPI, POR, XTAL, PLL, FIFO	None
RX	0x90	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+ADC, FIFO	RX Timer
TX	0xA0	go_tx	SPI, POR, XTAL, PLL,PA, FIFO	None

The time for switching between various states is listed in the table below.

Table 14. State Switching Time

	Destination State					
Source State	**SLEEP**	**READY**	**RFS**	**RX**	**TFS**	**TX**
SLEEP		660 us	770 us	820 us	770 us	820 us
READY	Immediately		110 us	160 us	110 us	160 us
RFS	Immediately	Immediately		20 us	Cannot switch	Cannot switch
RX	Immediately	Immediately	Immediately		Cannot switch	160 us
TFS	Immediately	Immediately	Cannot switch	Cannot switch		20 us
TX	Immediately	Immediately	Cannot switch	160 us	Immediately	

Notes:
In direct mode, if switching command is sent during transmission, it will exit Tx Immediately.
In packet mode, if switching command is sent during transmission, it will exit Tx after accomplishing current transmission.

The state transition and state code information is shown in the figure below.

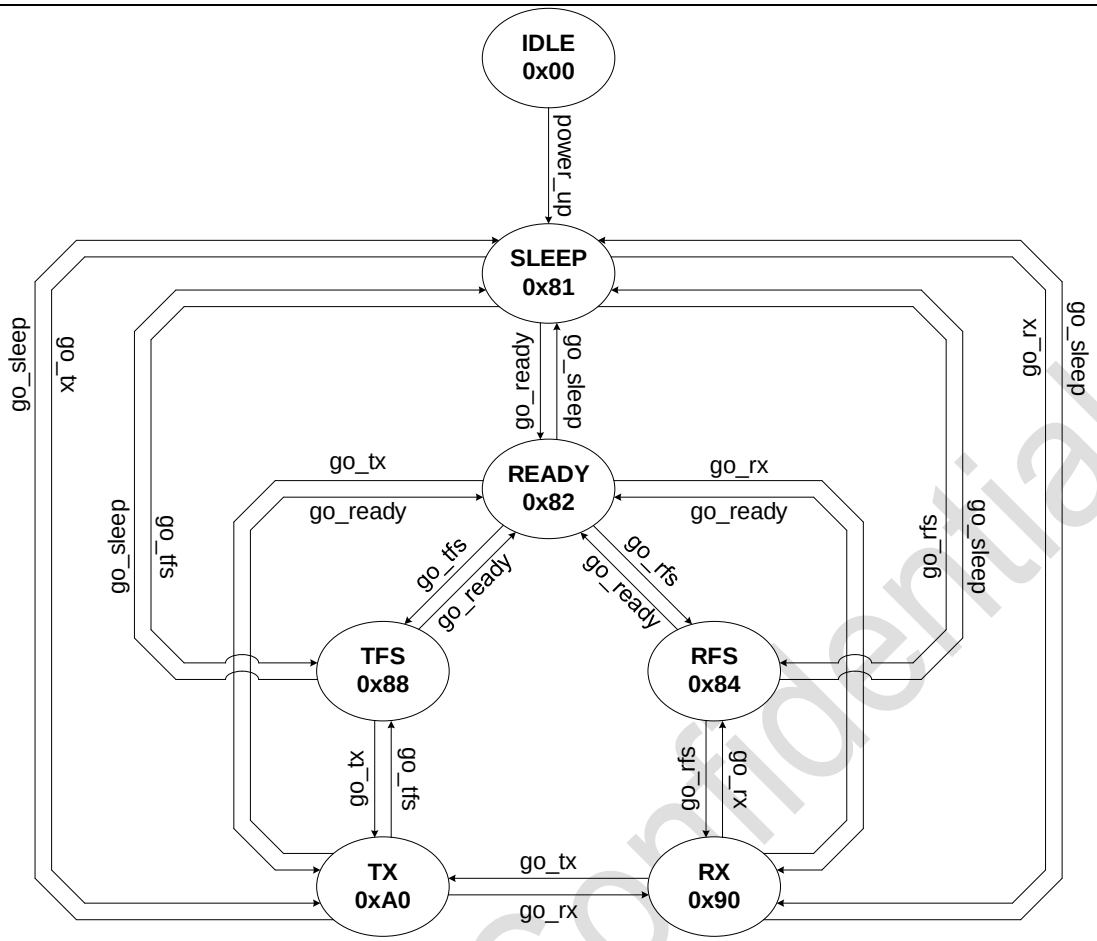


Figure 22. State Transition Diagram

- **SLEEP State**

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged.

However, the user cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

- **STBY State**

In STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased, and the FIFO can be operated. The user can choose whether to output CLKO (system clock) to PIN. Because the crystal and LDO is turned on, compared to the SLEEP, the time switching from the STBY to transmitting or receiving will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled. Switching from other state to STBY will be completed immediately.

- **RFS State**

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching from STBY to RFS probably requires PLL calibration and stability time of 110us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

- **TFS State**

TFS is a transition state before switching to TX. Except that the transmitter RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from

STBY to TFS probably requires PLL calibration and stability time of 110us. Switching from SLEEP to TFS needs to add the crystal start-up and settled time. Switching from other state to TFS will be completed immediately.

- **RX State**

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20us. Switching from STBY to RX needs to add the PLL calibration and settled time of 160us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 160us to switch successfully.

- **TX State**

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20us. Switching from STBY to TX needs to add the PLL calibration and settled time of 160us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 160us to switch successfully.

5.4 GPIO and Interrupt

The CMT2310A has 7 GPIO ports（GPIO0～GPIO5 and NIRQ）.Each GPIO can be configured as input or output independently. It also supports 3 interrupt ports, which can be configured to different GPIO outputs.

Table 15. CMT2310A GPIO

Pin #	Name	I/O	Function
23	GPIO0	IO	Can be configured as: DOUT, INT1, INT2, INT3, DCLK, TRX_SWT.
22	GPIO1	IO	Can be configured as: DCLK, INT1, INT2, DOUT, TRX_SWT.
14	GPIO2	IO	Can be configured as: INT1, INT2, INT3, DCLK, DOUT, ANTD1.
13	GPIO3	IO	Can be configured as: INT1, INT2, DCLK, DOUT, ANTD2.
7	GPIO4	IO	Can be configured as: DOUT, INT1, INT2, DCLK, CLKO, LFCLKO.
8	GPIO5	IO	Can be configured as: RSTn, INT1, INT2, DOUT, DCLK.
21	NIRQ	IO	Can be configured as: INT1, INT2, DCLK, DOUT, TCXO.

The interrupt mapping is listed in the table below. As INT1 and INT2 have the same mapping, it takes INT 1 as an example in the table below.

Table 16. CMT2310A Interrupt Mapping Table

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
INT_MIX	000000	Compounded interrupt, any one of the interrupts below is valid, INT_MIX will be valid.	Auto/By MCU
ANT_LOCK	000001	Interrupt for antenna lock being accomplished after antenna diversity function running.	By MCU
RSSI_PJD_VALID	000010	Interrupt for RSSI and/or PJD being valid.	Auto
PREAM_PASS	000011	Interrupt indicating successful receipt of Preamble.	By MCU
SYNC_PASS	000100	Interrupt indicating successful receipt of Sync Word.	By MCU
ADDR_PASS	000101	Interrupt indicating successful receipt of Addr.	By MCU
CRC_PASS	000110	Interrupt indicating successful receipt and CRC check being passed.	By MCU
PKT_OK	000111	Interrupt indicating receipt of an entire and correct packet.	By MCU
PKT_DONE	001000	Indicates that the current data packet has been received with the occurring of one of the 4 cases below. 1. A complete and correct packet is received. 2. Manchester decoding error occurs and the decoding circuit restarts automatically. 3. NODE ID receiving error occurs and the decoding circuit restarts automatically. 4. A signal conflict is found and the decoding circuit does not restart automatically but waits for the MCU to process.	By MCU
SLEEP_TMO	001001	Interrupt indicating SLEEP timer timeout.	By MCU
RX_TMO	001010	Interrupt indicating RX timer timeout.	By MCU
RX_FIFO_NMTY	001011	Interrupt indicating RX FIFO being empty.	Auto
RX_FIFO_TH	001100	Interrupt indicating the unread content of RX FIFO exceeding FIFO TH.	Auto
RX_FIFO_FULL	001101	Interrupt indicating RX FIFO being full	Auto
RX_FIFO_WBYTE	001110	Interrupt generated every time a BYTE is written into RX FIFO, i.e., it is a pulse.	Auto

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
RX_FIFO_OVF	001111	Interrupt indicating RX FIFO being overflow	Auto
TX_DONE	010000	Interrupt indicating TX completion.	By MCU
TX_FIFO_NMTY	010001	Interrupt indicating TX FIFO not being empty.	Auto
TX_FIFO_TH	010010	Interrupt indicating the unread content of TX FIFO exceeding FIFO TH.	Auto
TX_FIFO_FULL	010011	Interrupt indicating TX FIFO being full.	Auto
STATE_IS_READY	010100	Interrupt indicating that the current state is READY.	Auto
STATE_IS_FS	010101	Interrupt indicating that the current state is RFS or TFS.	Auto
STATE_IS_RX	010110	Interrupt indicating that the current state is RX.	Auto
STATE_IS_TX	010111	Interrupt indicating that the current state is TX.	Auto
LBD_STATUS	011000	Interrupt indicating that low voltage detection being active (VDD is lower than the set TH).	By MCU
API_CMD_FAILED	011001	Interrupt indicating API command execution error.	By MCU
API_DONE	011010	Interrupt indicating API command completion.	By MCU
TX_DC_DONE	011011	Interrupt for Duty Cycle TX mode complete	By MCU
ACK_RECV_FAILED	011100	Interrupt indicating ACK receiving failure.	By MCU
TX_RESEND_DONE	011111	Interrupt for repeated TX complete	By MCU
NACK_RECV	011110	Interrupt indicating receipt of NACK.	By MCU
SEQ_MATCH	011111	Interrupt indicating successful serial number matching.	By MCU
CSMA_DONE	100000	Interrupt for CSMA complete	By MCU
CCA_STATUS	100001	Signal channel sensing interrupt.	By MCU

By default, Interrupt is enabled when register value is 1. Users can set the INT_POLAR register bit to 1to make all interrupts to be enabled when the register value is 0. Take INT1 as an example, the control andselection of two different types of interrupt sources is shown in the figure below. The control and mapping ofINT1 and INT2 is the same and both can be mapped to any GPIO.INT_MIX is the only source for INT3, which can only be mapped to GPIO0 and GPIO2. In application, users can choose either to map all interrupt sources to the interrupt port through INT_MIX (identify which interrupt is valid by checking the interrupt flag) or directly map a specific interrupt source to the interrupt port.

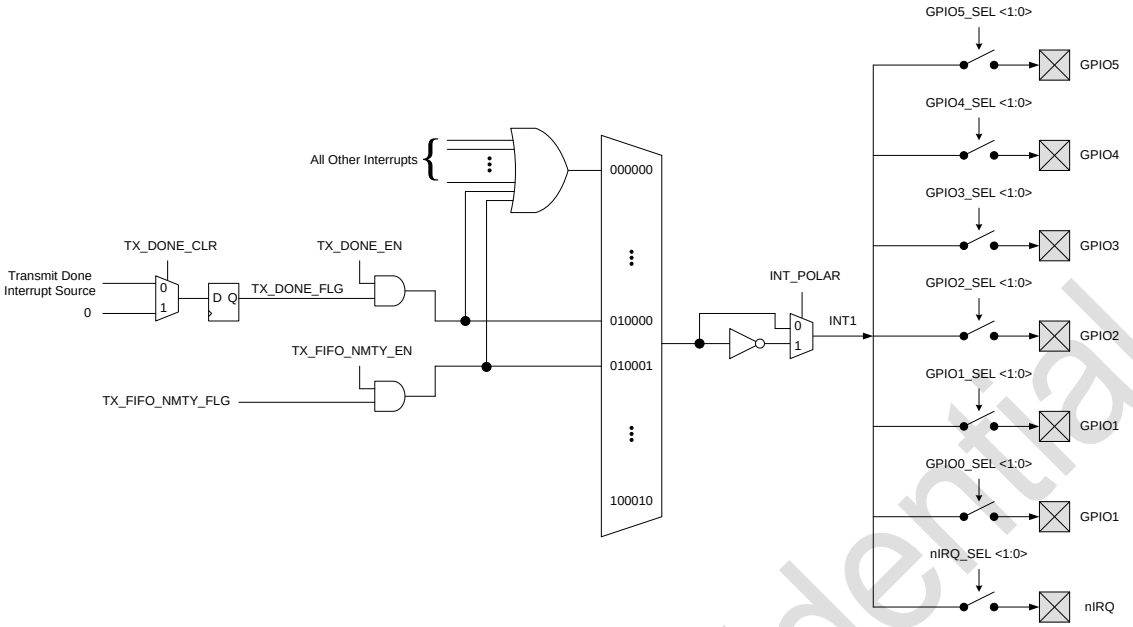


Figure 23. CMT2310A INT1 Interrupt Mapping Diagram

6 Data Packet and Packet Handler

Data mode specifies how the MCU inputs transmission data and acquires received data. The CMT2310A supports both direct Rx mode and packet mode.

- Direct Rx Mode - In Rx mode, it only supports preamble and sync detection, namely FIFO does not work;
- Packet Mode – it supports all packet formats and FIFO.

6.1 Direct Rx Mode

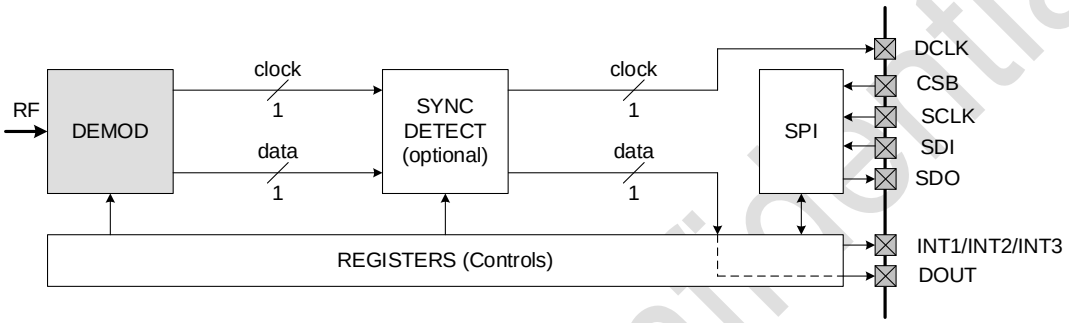


Figure 24. Direct Mode Data Path

Rx processing

In direct mode, the data from the demodulator is sent directly to the external MCU via the DOUT pin. DOUT can be set as GPIO1-GPIO5 and NIRQ.The typical RX direct mode control sequence for the MCU is shown as follow:

1. Configure GPIO through register CUS_IO_SEL.
2. Configure DATA_MODE = 0.
3. Send the go_rx command.
4. Capture the data from DOUT continuously.
5. Send the go_sleep/go_stby/go_rfs command to complete receiving and meanwhile to save power.

6.2 Packet Mode

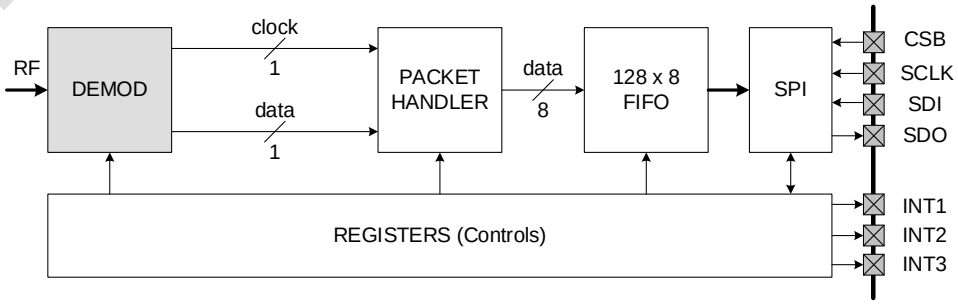


Figure 25. Packet Mode Data Path

The CMT2310A supports identical packet configuration for both Tx and Rx. It provides both the classic packet formats and more flexible packet formats, including variable packet format with Length located before Node ID, variable packet format with Length located after Node ID, and fixed packet format. Each element in the packet supports flexible configuration is shown in the figure below.

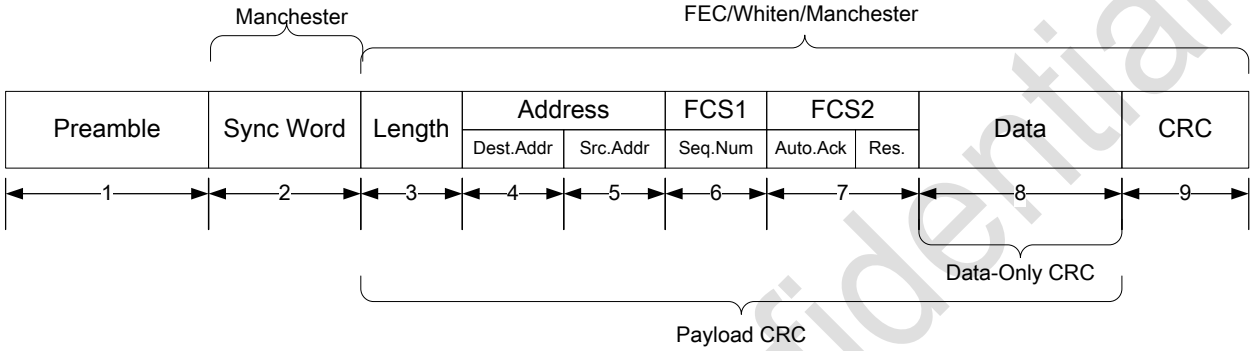


Figure 26. CMT2310A Packet Format

6.2.1 Rx processing

In the packet mode, the output data from the demodulator will be transferred to the packet handler for decoding, and then filled in the FIFO.The packet handler provides a variety of decoding mechanisms and options to determine the validity of the data, which can reduce the workload of the MCU.The typical Rx sequence in packet mode for the MCU is:

1. Configure GPIO through register CUS_IO_SEL.
2. Select the interrupts to be output.
3. Send go_rx command.
4. Read RX FIFO according to related interrupt status.
5. Send go_sleep/go_stby/go_rfs command tocomplete receiving and meanwhile to save power.
6. Clear interrupts.

6.2.2 Tx processing

In packet mode, the MCU must pre-loaded the FIFO with data in READY and TFS states, and then send the go_tx command to send the data out.The typical Tx packet mode control sequence for the MCU is shown as below:

1. Configure GPIO through register CUS_IO_SEL.
2. Sendgo_ready and fill data into FIFO.
3. Select the interrupts to be output.
4. Send go_tx command.
5. Write the data into FIFO according to the related interrupt status.

6. Exit to the selected state automatically after finishing transmission of N packets without sending any command.

Generally, the FIFO, packet handling mechanism and the related rich interrupt resources of the CMT2310A are compatible with most products of the same type in the market and can communicate with them seamlessly. Please see RPPDK configuration GUI for more details.

7 Low Power Operating

7.1 Duty Cycle Operating Mode

The CMT2310A allows Duty Cycle mode operating for both Tx and Rx by configuring related registers for power saving purpose.

The Rx Duty Cycle includes 5 modes as follows.

1. Fully manual mode.
2. Automatic wake-up from sleep, then switch to manual control.
3. Automatic wake-up from sleep, then enter Rx and then exit Rx manually.
4. Automatic wake-up from sleep, then enter Rx and then exit Rx automatically.
5. Fully automatic mode.

The Tx Duty Cycle includes 3 modes as follows.

1. Manually enter TX, then automatically exit TX
2. Automatic wake-up from sleep, then switch to manual control.
3. Fully automatic transmission.

7.2 Super-low Power (SLP) Rx Mode

The CMT2310A provides a series of options helping users achieving super-low power (SLP) Rx to meet different application requirements. All these options are available only when RX_TIMER_EN is set as 1, namely Rx counter is active. The main purpose of SLP Rx is to minimize Rx time when no signal is received meanwhile properly extend Rx time when valid signal is received, thus to accomplish stable data receive with minimum power consumption.

In general, traditional short-range wireless transceiver systems apply the solution as shown in the figurebelow to fulfill low-power transceiver. The CMT2310A supports this fundamental solution as well. Moreover, based on this solution, the CMT2310A extends 13 solutions with more favorable power consumption performance. The fundamental solution is detailed as follows.

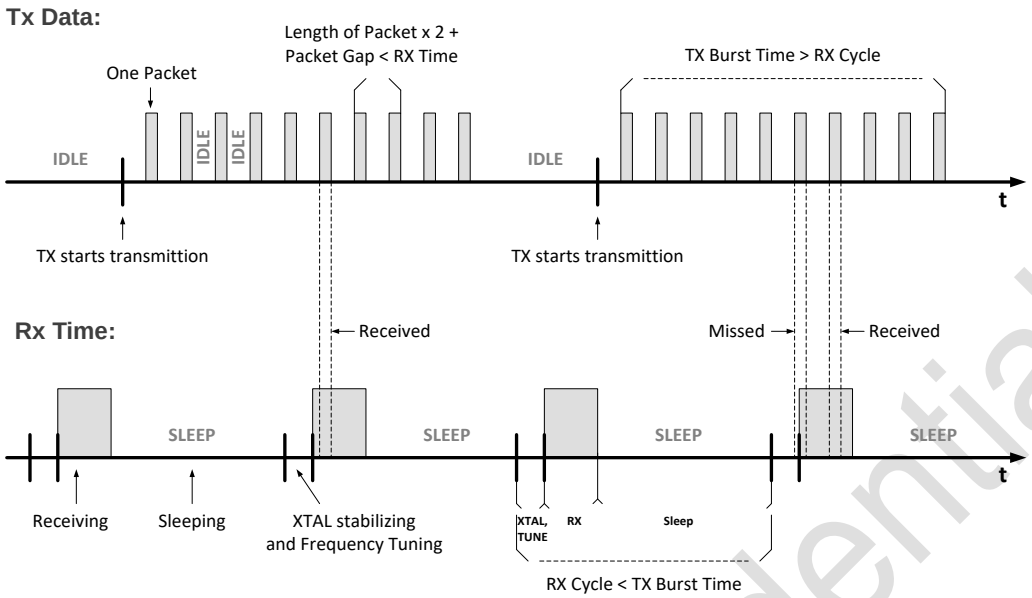


Figure 27. Fundamental Low-power Receiver Scheme

The traditional low-power transceiver solution and the 13 extended low-power solutions based on it are listed in the table below.

Table 17. Low-power Rx mode

No.	Rx ExtendedMethods	Rx ExtendedCondition
0	No Rx extension is supported.Exit Rx state as soon asT1 is timeout.	None
1	Once meet the Rx extended condition during T1, leave T1 and hand over control to the MCU.	RSSI_VLD is valid.
2		PREAM_OK is valid.
3		RSSI_VLD and PREAM_OK are valid at the same time.
4	Once detect RSSI_VLD =1during T1, leave T1 and stays in Rx state, then exit Rx state until RSSI is not valid.	RSSI_VLD is valid.
5	Once meet the Rx extended condition during T1, switch to T2.Exit Rx as soon as T2 is timeout.	RSSI_VLD is valid
6		PREAM_OK is valid
7		RSSI_VLD and PREAM_OK are valid at the same time.
8		Anyone of PREAM_OK or SYNC_OK is valid.
9		Anyone of PREAM_OK or NODE_OK is valid.
10		Anyone of PREAM_OK or SYNC_OK or NODE_OK is valid.
11	Once meet the Rx extended condition during T1, switch to T2.Leave T2 and handover control to MCU as soon as SYNC is detected, otherwise exit Rx whenT2 is timeout.	RSSI_VLD is valid.
12		PREAM_OK is valid.
13		RSSI_VLD and PREAM_OK are valid at the same time.

Notes:

The signal source of RSSI_VLD can be the RSSI comparison result or PJD detection result or both of them being valid.

The T1 and T2 mentioned in the table above refer to the RX T1 and the RX T2 time interval that can be set via the registers or RFPDK.The source of RSSI_VLD can be the comparison result of the RSSI or the detection result of the phase jump detector (PJD).

7.3 Rx Automatic Frequency Hopping (RX AUTO HOP)

When the chip enters a channel for receiving, if no successful events are detected in the corresponding mode, the chip will return to READY or RFS state according to FREQ_SW_STATE, then automatically configure the channel value in the next byte in the hopping table then re-enter Rx state for receiving. If the automatic switched state is READY, the PLL frequency will be re-calibrated before re-entering RX with corresponding calibration time consumed; if the automatic switched state is RFS, the PLL frequency will not be re-calibrated, thus the switching time is shorter. If the interval between any two frequency points in the frequency hopping table exceeds 2MHz, it is recommended to configure FREQ_SW_STATE to the READY state, for it is necessary to recalibrate the PLL in this case.

If successful events are detected, the chip will auto-hop and wait for the further processing from the external MCU or switch to the pre-configured state. If successful events are detected when the entire table hopping is finished, the chip will hop from the start of the table if RX_HOP_PERSIST is configured as 1, or else return to the state specified in RX_EXIT_STATE if RX_HOP_PERSIST is configured as 0 to finish the Rx-auto-hopping operation. The destination frequency point calculation is as follows.

FREQ = 1K x FREQ_SPACE<7:0> x FREQ_CHANL<7:0>

In the calculation above, FREQ_SPACE<7:0> is an independent register, FREQ_CHANL<7:0> is configured through 64 registers with each one stores a single channel value.

The register REQ_CHANL_LV of RX_Auto_Hop mode lets users know which channel currently is used. Moreover, the register FREQ_DONE_TIMES is to let users read the number of currently finished hopping.

The RX_Auto_Hop mode needs to use RX T1 TIMER and RX T2 TIMER, therefore TIMER_RX_EN must be set to 1. RX T1 TIMER is configured through TIMER_M_RX_T1 and TIMER_R_RX_T1 and the actual timer time is calculated according to the timer formula. RX T2 TIMER is configured through TIMER_M_RX_T2 and TIMER_R_RX_T2 and the actual timer time is calculated according to the formula.

CCA_INT_SEL is used to determine whether RSSI_PJD_VLD is judged through RSSI or PJD; RX_EXIT_STATE is used to determine which state to be returned to when it exits Rx; PKT_DONE_EXIT_EN is used to determine when receiving PKT_DONE whether it will exit Rx and return to the state configured by RX_EXIT_STATE or keep in the current state.

After having configurations done, users can set RX_AUTO_HOP_EN to 1 to enable the function, then send command go_rx to enter the RX_Auto_Hop mode. During the auto-operation, if events triggering the stop of the auto-operation occur, the chip will stop the auto-operation and stay in some fixed state. If requiring to stop the RX_Auto_Hop operation, users can set API_STOP to 1. When the chip detects this bit being set, it will set API_DONE_FLAG to 1 upon the next state switching, then keep the current configurations, exit the RX_Auto_Hop function and return to READY state.

After the halt of RX Auto Hop, if RX_AUTO_HOP_EN is kept as 1, the chip will enter Rx-auto-hopping operation again once users send go_rx command again, and it will start hopping from the next frequency point since the latest finished hopped frequency point. If users wanted start hopping from the first frequency point, they can clear register FREQ_DONE_TIMES before sending go_rx command.

The Rx-Auto-Hop supports the following 7 operating modes.

Table 18. Rx-Auto-Hop Operating Mode

No.	Rx Extension Mode	Rx Extension Condition
0	If it is set to 0, there's no Rx extension. If PKT_DONE is detected before T1 is timeout and PKT_DONE_EXIT_EN = 1, it exits auto-hopping and switches to the state specified by RX_EXIT_STATE. Otherwise, it exits Rx when T1 is timeout and returns to the state specified by FREQ_SW_STATE then continue to hop the next frequency point.	None
1	If it meets detection conditions within T1, it exits from T1 and hands over control to the MCU (and keeps the state); if it does not meet detection conditions within T1, it exits Rx when T1 is timeout and returns to the state specified by register FREQ_SW_STATE and continue to hop the next frequency point.	RSSI_PJD_VLD is valid.
2		PREAM_OK is valid.
3		RSSI_PJD_VLD and PREAM_OK are valid at the same time.
4	If it meets detection conditions within T1, it switches to T2; otherwise if it does not meet detection conditions and timeout occurs, then it exits Rx and returns to the next frequency point. If it detects SYNC within T2, it exits from T2 and hands over control to the MCU (and keeps the state); otherwise it exits Rx when T2 is timeout and returns to the state specified by register FREQ_SW_STATE and continue to hop to the next frequency point.	RSSI_PJD_VLD is valid.
5		PREAM_OK is valid.
6		RSSI_PJD_VLD and PREAM_OK are valid at the same time.

7.4 TX Automatic Frequency Hopping (TX AUTO HOP)

In TX Auto Hop, FREQ_TIMES<7:0> is used to configure the size of the frequency hopping table. The table provides up to 64-byte space for users to store user configured signal channel information. The frequency hopping process is as follows.

The chip enters a channel to transmit. After the transmission is accomplished, the chip returns to either the READY or TFS state according to FREQ_SW_STATE;it automatically configures the channel value of the next byte in the frequency hopping table, and then re-enters the TX state to transmit.During the process, if the automatically switched status is *READY*,PLL frequency is re-calibrated before re-entering *TX with* corresponding calibration time consumed*;* otherwise if the automatically switched status is *TFS,*there's no PLL frequency re-calibration, thus switching time being shorter. If the interval between any two frequency points in the frequency hopping table exceeds 2MHz, it is recommended to configure FREQ_SW_STATE to the *READY* state, for it is necessary to recalibrate the PLL in this case.

When it finishes the entire table hipping, if RX_HOP_PERSIST is configured as 1, the chip will continue to hop the table from the beginning; otherwise, if RX_HOP_PERSIST is configured as 0, it will return to the TX_EXIT_STATE state and stop the operation of automatic frequency hopping transmission. The formula to calculate the target frequency in frequency hopping is as follows.

FREQ = 1K x FREQ_SPACE<7:0> x FREQ_CHANL<7:0>

Where, FREQ_SPACE<7:0> is an independent register, and FREQ_CHANL<7:0> is configured by 64 registers, each storing one channel value.

The TX_Auto_Hop mode provides the register REQ_CHANL_LV to let users know the current channel value. Moreover, the register FREQ_DONE_TIMES is for users to read the number of currently completed frequency hopping.

When making the configurations ready, users can set TX_AUTO_HOP_EN to 1 to enable the function, then send the go_tx command to enter the TX_Auto_Hop mode. If requiring to stop the TX_Auto_Hop function forcedly, users can set API_STOP to 1; then the chipdetects this bit and subsequently upon the next state switching it sets API_DONE_FLAG to 1 with retaining the current configurations, thereby, it exits TX_Auto_Hop and returns to the READY state.

7.5 Automatically Re-sending (TX AUTO RESEND)

The automatic re-sending function is an automatic control mechanism to realize the handshake between the transmitter and the receiver. It provides two packet format fields, SEQNUM and FCS2,to judgeif the handshaking between transmitter and the receiver succeeds. These two fields are part the packet, and need to be enabled by SEQNUM_EN and FCS2_EN when the function is used.

Its implementation principle is that: the transmitter configures the local SEQNUM and sets the NACK bit in the FCS2 field to 1 for transmission; after the transmission is accomplished, it enters the RX state and waits for the response; when it receives the response and finds the SEQNUM in the response packet matches the local SEQNUM and the received NACK bit is 1, the handshaking is recognized successful.

At the receiver side, after enabling the ACK function, it enters the RX state. When the packet is receivedsuccessfully, the receiver judges whether need to answer it by the received NACK bit. If a response is needed, it enters the TX state, and the received sequence numberand NACK bit are sent back. The PKT_DONE interrupt is generated after sending back operation is completed; then it either returns back to the state configured in RX_EXIT_STATE or remains in the RX state according to PKT_DONE_EXIT_EN.

7.6 Carrier Sensing Multi-path Accessing (CSMA)

CSMA is a kind of conflict avoidance mechanism (speaking after sensing), that is, before transmission it senses the channel idle status first, then determine whether to transmit or not, which helps to avoid the potential conflicts when multiple transmitters use the same channel and increase the possibility of successful packet receiving for receivers. The key point of CSMA is comparing the RSSI with the specified threshold to judge the channel idle status. When the channel is busy, it will repeat the procedure from back-off to listening for several times until it finds the the channel in idle. If it fails to detect channel being idle when reaching the repeated time limit, the corresponding interrupt and flag will be generated and transmission will be stopped. During back-off procedure, the chip stays in SLEEP state. In the PERSISTENT mode, it will back to RFS state first and then switch to Rx state for listening rather than back to SLEEP state. If it was under non-PERSISTENT mode, the maximum number of non-idlechannels can be configured by the CSMA_TIMES. While as if the channel was still busy, it will exit the CSMA and return to the READY state.

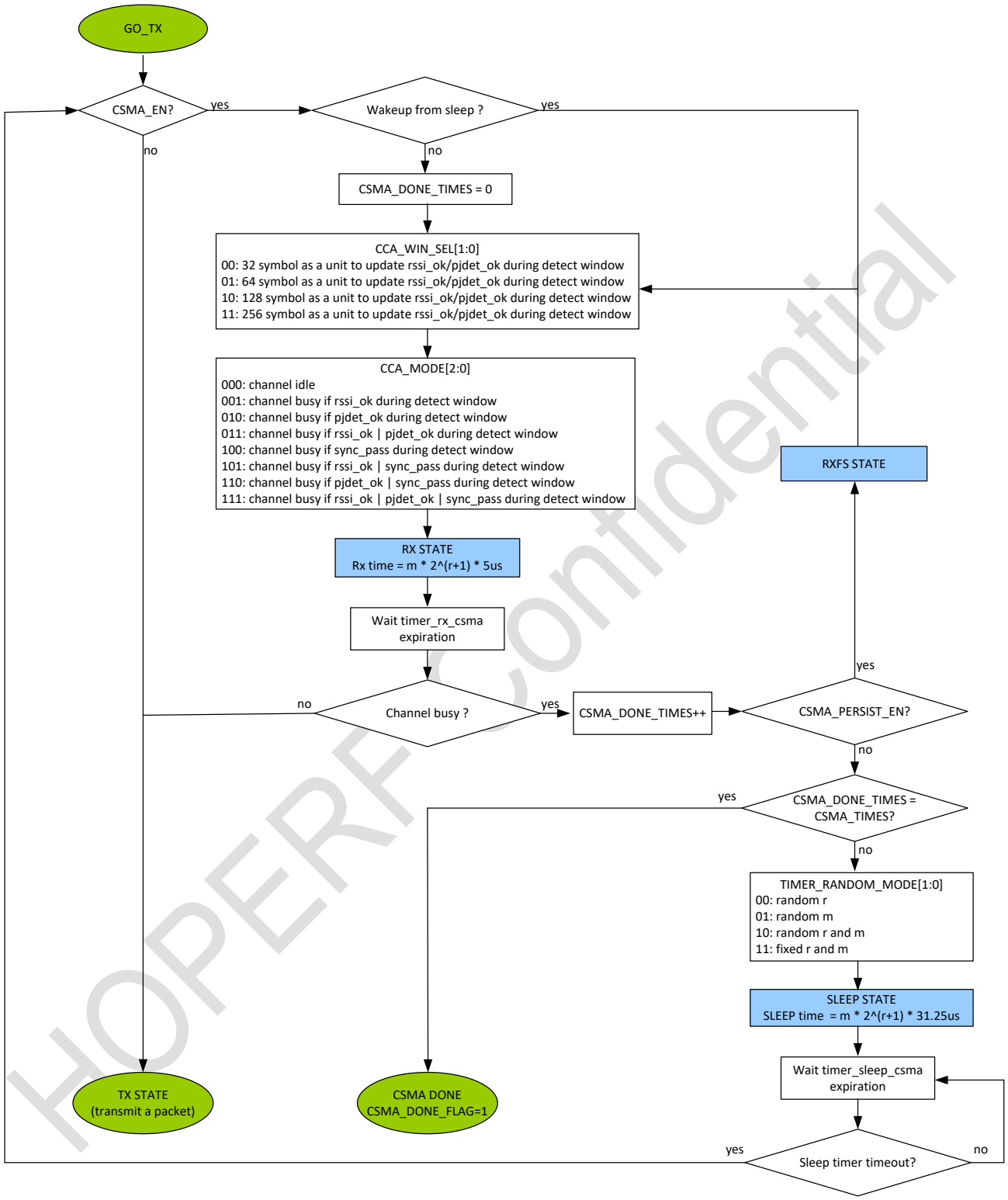


Figure 30. Operation Process of Carrier Sensing Multi-path Accessing

7.7 Antenna Diversity

Throughout RF transmission paths, both inter-impact among direct waves, reflected waves, and scattered waves generated by various objects (namely multi-path fading), and Doppler shift (the wavelength of the object radiation varies due to the relative motion between the wave source and the observer) would cause signal loss. A targeting solution for this is the diversity technology. The diversity technology can be categorized into space diversity, polarization diversity, angle diversity, frequency diversity, and time diversity. The CMT2310A applies the dual-antenna angle diversity technique, which allows electromagnetic waves to pass through two different paths at different angles to reach the receiver end. The CMT2310A receiver determines which path is chosen to receive data packets by using RSSI to compare the signal-to-noise ratios of the two paths.

Users can configure the register ANT_DIV_MANU as 0 to make the CMT2310A automatically switch and lock the antenna. Users can configure ANT_DIV_EN as 1 to enable the antenna diversity function. ANT_SW_DIS is configured as 0 when the locking conditions are met while switchingscan of the two antennas. It will lock the antenna with the larger RSSI value by comparing the RSSI values of the two antennas. Configuring ANT_SW_DIS as 1 means that, if the current RSSI value is found to be 16 dB higher than the RSSI_Compare_TH value set by the RFPDK (the register is RSSI_ABSOLUTE_TH), while switching and scanning between the two antennas, the current antenna is locked and switching stops then; otherwise, the RSSI values of the two antennas are compared and one of the antennas is locked then.

Users can also set the ANT_DIV_MANU register to 1 to manually control the antenna diversity switch. When ANT_SELECT is set to 0, GPIO2 outputs 1 and GPIO3 outputs 0. When ANT_SELECT is set to 1, GPIO2 outputs 0 and GPIO3 outputs 1.

The application schematic diagram for the direct-tie direct matching network as recommended applying antenna diversity transceiver is shown in the figure below. The two antennas are placed at right angle. The antenna switches are controlled automatically by GPIO2 and GPIO3. When GPIO2 outputs 1, GPIO3 outputs 0, the antenna controlled by GPIO2 is selected then. On the contrary, when GPIO2 outputs 0, GPIO3 outputs 1, the antenna controlled by GPIO3 is selected then. Each antenna switch will cause anoise figure of the receiver at about 0.5 dB.

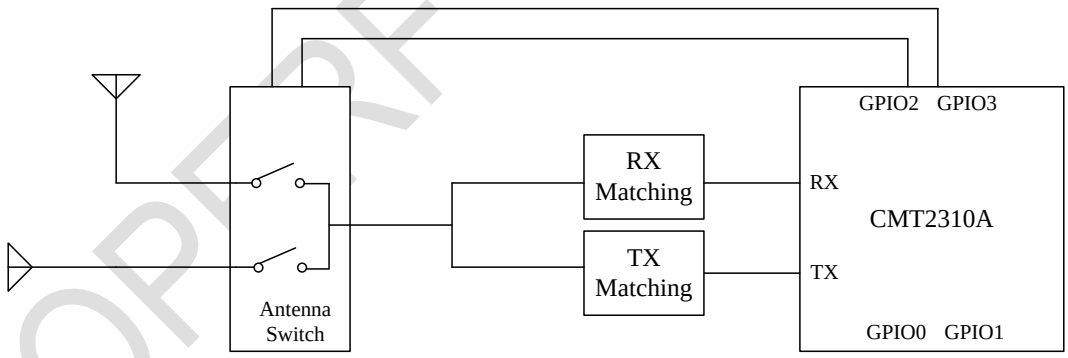


Figure 31. Transceiver Application Schematic Diagram Applying Antenna Diversity with Direct-tie Matching Network

If a design with separated matching networks for receiving and transmitting is required as shown in the figure below, users can add an antenna switch controlled by GPIO0 and GPIO1 and configure TRX_SWITCH_EN = 1 to enable the TRX switch. When TRX_SWITCH_INV = 0, GPIO0 outputs 1 and GPIO1 outputs 0 in RX state with; and GPIO0 outputs 0 and GPIO1 outputs 1 in TX state. If TRX_SWITCH_INV = 1, the above output values reverse.

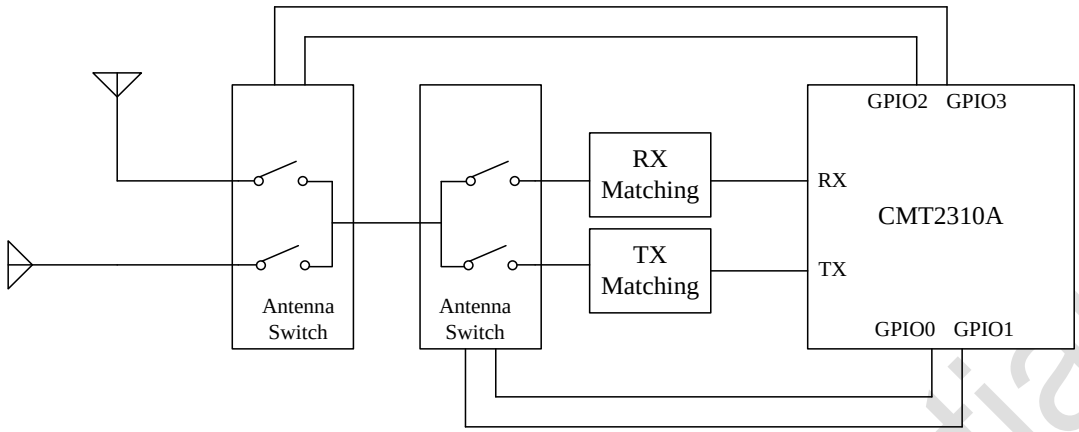


Figure 32. Transceiver Application Schematic Diagram Applying Antenna Diversity with Separated Matching Network

ANT_LOCK_EN is the enabling bit of the diversity antenna lock interrupt. ANT_LOCK_FLAG is the antenna lock flag bit. ANT_LOCK_CLR is the antenna lock interrupt flag clear bit.Users can read the value on the register ANT_INSTR to know which antenna is automatically locked to the current antenna diversity when the antenna locked. If ANT_INSTR is 0, it will lock the GPIO2= 1&GPIO3 =0 connected antenna; otherwise, it will be GPIO2= 0&GPIO3 =1.

Users can also read the RSSI values of the two antennas after the lock by using the RSSI_VALUE and RSSI_MIN_VALUE registers. RSSI_VALUE is the large value while RSSI_MIN_VALUE is the small one. It is recommended that users select sync_ok for RSSI Detect Mode in the RFPDK Feature 2 Settings page, so that the locked antenna will update the RSSI value to the RSSI_VALUE after sync_ok.

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8 User Register

All configuration and control operations from external MCU are accomplished by accessing the registers in the 3 pages through SPI interface. Shifting among the 3 pages will be accomplished through writing the address 0x7E. As shown in the table below, the address range 0x00 ~ 0x71 are divided into 3 banks for understanding purpose, configuration bank (including 6 sub-banks), control bank 1 and control bank 2, which will be detailed below.

The addresses of the 3 banks are continuous. Operation method against the 3 banks have no essential difference, namely all operations are direct read/write operations following the SPI register read/write timing. However, for the 3 banks the functionalities and usage are different as shown in the table below.

Table 19. CMT2310A Register Bank Partitioning

Page	Address	Bank	Function Description
0	0x00 - 0x0F	System control bank 1	For chip operation and control like state switching, status checking, etc.
	0x10 - 0x17	System control bank 2	For chip function enabling.
	0x18 - 0x27	Interrupt Control bank	For reading and clearing interrupt flag, unaccessible in SLEEP state.
	0x28 - 0x5F	Configuration bank (packet format)	For packet format and FIFO related configurations.
	0x60 - 0x77	Configuration bank (system feature)	For system operating related function configurations.
1	0x00 - 0x0F	Configuration bank (CMT internal use)	For CMT internal use only.
	0x10 - 0x27	Configuration bank (Tx)	For transmitter related feature configurations.
	0x30 - 0x68	Configuration bank (Rx)	For receiver related feature configurations.
2	0x00 - 0x3F	Configuration bank (auto- frequency hopping)	For storing automatic channel hopping table information.

Notes:

1. In Page 0, address 0x7A is FIFO accessing interface address, address 0x7B is the interface for continuously accessing register.
2. In all Pages, address 0x7E is the interface for Page shifting.
3. In all Pages, address 0x7F is the interface for software reset.
4. The addresses unlisted in the table are inaccessible.

Except the interrupt configuration bank, all banks can be accessed in SLEEP state and the configuration data will retain if no POR reset or power down occurs.

The register values in Page 0 and Page 1 can come either from RFPDK or from user application based on actual requirements. In general, except a few parameters about RF frequency or data rate that may require configuring for multiple times in user application, most of the registers just need to configure once in the initial stage.

As for the frequency hopping table in Page 2, users need to have specific design and configuration according to the guidance in related AN document.

9 Ordering Information

Table 20. CMT2310A Ordering Information

Model	Description	Packaging	Package	Operating Condition	Minimum Order Quantity
CMT2310A-EQR [1]	CMT2310A, ultra-low power sub-1GHz RF transceiver	QFN24 (4x4)	Tape and Reel	1.8 to 3.6V, -40 to 85 ℃	3,000 pcs

Notes:

[1]. E refers to extended Industrial product rating, which supports temperature range from -40 to +85 °C.
Q refers to the package type QFN24 4x4.
R refers to tape and reel type, and the minimum ordering quantity (MOQ) is 3,000 pieces.

Please visit www.hoperf.com for more product/product line information.

Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

10 Packaging Information

The packaging information of the CMT2310A is shown in the figure below.

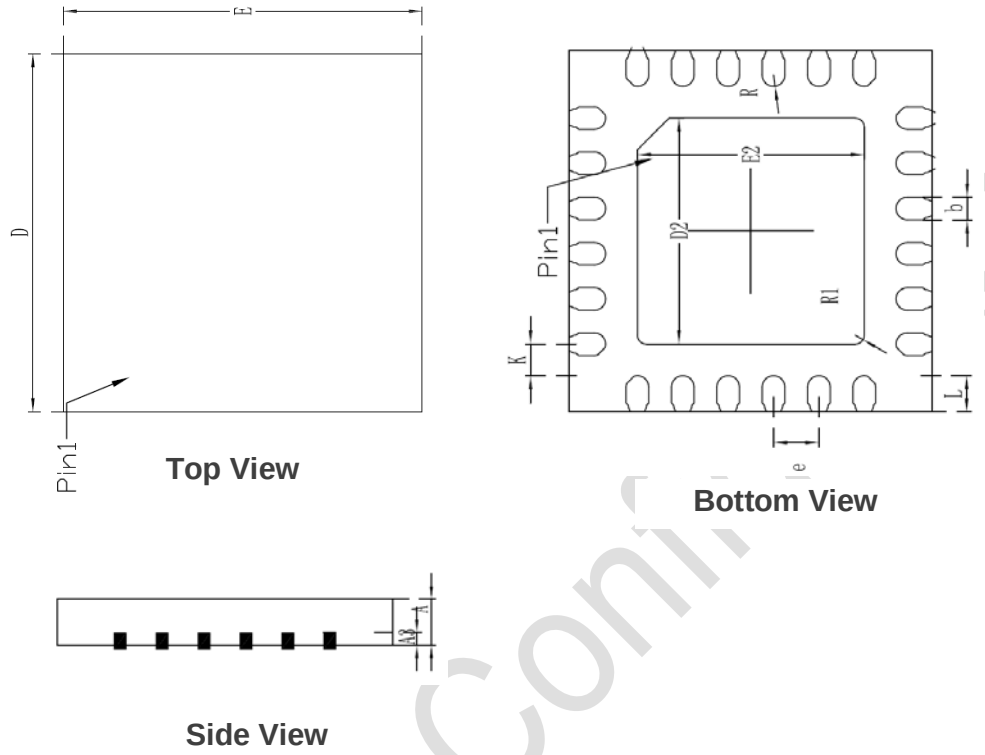

Figure 33. 24-Pin QFN 4x4 Packaging

Table 21. 24-Pin QFN 4x4 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0,02	0,05
A3	--	0.15	--
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40	0.50	0.60
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.20	0.30	0.40
K	0.20	--	-
R	--	0.10	-
R1	-	0.10	-

11 Top Marking

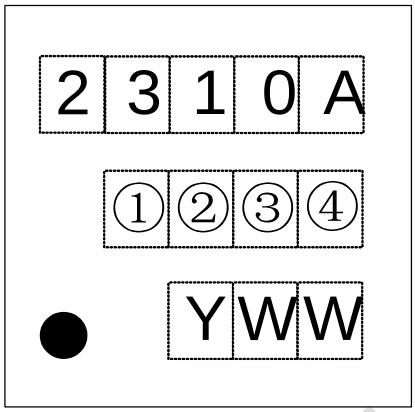

Figure 34. CMT2310A Top Marking

Table 22. CMT2310A Top Marking Information

Marking method	Laser.
Pin 1 mark	Diameter of the circle = 0.3 mm.
Fontsize	0.5 mm, align right.
Line 1 marking	2310A, refers to model CMT2310A.
Line 2 marking	①②③④is internal tracing code.
Line 3 marking	YWW is the date code is assigned by assembly factory. Y represents the last digit of the year. WW represents working week.

12 Revise History

Table 23. Revise History Records

Version No.	Chapter	Description	Date
1.0	All	Initial version	2021-12-21
1.0A	All	Ready for review	2022-01-09
1.0B	All	1. Update pin name NSEL to CSB. 2. Update parameter name SCL to SCLK. 3. Change the note information in Table 21 in section 8.1. 4. Change frequency deviation range in table 6 in section 1.6. 5. Change packaging size values in table 23 in section 10. 6. Some update based on review comments.	2022-01-18
1.0C	All	1. Update SPI interface parameter values in the table 12 in section 1.12. 2. Update 0x7B as the operation port of BRW in 5.1.2. 3. Update 0x7A as the operation port of FIFO in 5.2.1. 4. Modify SPI Sequence Chart in 5.1.2； 5. CMSA description modified and operating process added in 7.6.	2022-01-19
1.0D	5	1. 5.4 GPIO and interrupt，GPIO number changed to 7； 2. Update TFS and TX status arrows descriptions in figure 5.16；	2022-01-20
	3	Update the BOM figure	2022-02-14
	7	7.7 Update the description of Antenna Diversity	2022-02-14
	1.4	Adding the CCR Indicator	2022-03-08
1.0E	5	1. 5.3 The function description of TX_RESEND_DONE is changed to "Interruption for repeated transmission complete" 2. 5.3 The CSMA_DONE function description is changed to CSMA operation interruption complete. 3. 5.3 The function description of TX_DC_DONE is changed to "Duty Cycle tx interruption complete. 4. 5.1 Update the description of SPI Burst at the top of page 27. 5. Remove the function of LFXO1 and LFXO2 at Table 18	2022-03-14
	6	6.2.2 The description of Tx processing changed to " In packet mode, the MCU must pre-loaded the FIFO with data in READY and TFS states, and then send the go_tx command to send the data out."	2022-03-14
	1	Delete the electrical characteristic description of low frequency crystal at 1.10.	2022-03-14

1.0F	1	1.1.3 Current data update at the RF power consumption table.	2022-04-19
	10	Update package data	2022-07-18
2.0	10	Update package data	2022-07-28
2.1	5.2.1	Update the first FIFO access address in Figure 17/18/19/20	2022-10-14
2.2	1	1.4 Added the saturation input signal level	2022-11-16
2.3	6	Delete direct Tx mode	2023-04-26
2.4	5.3.2	Update the state switching time in description part	2023-05-18
	1.4	Change the Unit of Co-channel rejection，Adjacent channel rejection，Blocking，Image Rejection from dBc to dB.	

13 Contacts

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