HOPERF

CMT2390F64

Ultra-low Power Sub-1GHz Wireless Transceiver

MCU Features

- A 32-bit general-purpose micro-controller based on the Arm® Cortex®-M0 core，single cycle hardware multiply instrction
- Up to 64 KByte on-chip Flash
  - supports encrypted storage and hardware ECC verification
  - endurance more than 100,000 cycles, 10 years of data retention
- 8 KByte on-chip SRAM，supports hardware parity
- Programming method：
  - SWD online debugging interface
  - UART Bootloader
- 23 general IO (4 with SPI multiplexing in RF part)
- Low-power management：
  - Stop mode: RTC Runs, maximum 8 KByte SRAM retention, CPU register retention, all IO retention
  - Power Down mode (PD): supports 3 IO wakeup
- Clock：Up to 48 MHz
  - LSE：32.768 KHz，external low-speed crystal
  - HSI：Internal high-speed RC OSC 8 MHz
  - LSI：Internal low-speed RC OSC 30 kHz
  - Built-in high-speed PLL
  - One channel clock output, which can be configured as configurable system clock, HSI or PLL post-divided output
- Reset
  - Supports power-on/power-down/external pin reset
  - Supports programmable low voltage detection and reset
  - Supports watchdog reset
- Communication Interface
  - 3 x UART interface, with a maximum rate of 3 Mbps, of which 2 USART interfaces support 1xISO7816 , 1xIrDA, LIN,1 of which supports low power consumption (LPUART）, the highest communication rate in this mode is 9600bps and stop mode can be awakened.
  - 2 x SPI, the rate is up to 18 MHz, one of which supports multiplexing with I2S
  - 2 x I2C, the rate is up to 1 MHz, master-slave mode is configurable, and dual-address response is supported in slave mode
- Analog interface
  - 1 x 12 bit high-speed ADC, 1 Msps, up to 6 external single-ended input channels
  - 1 x OPAMP, built-in programmable gain amplifier up to 32 times
  - 1 x COMP, built-in 64-level adjustable comparison benchmark
  - 1x high speed 5-channel DMA control, source address and destination address can be configured arbitrarily
- Timer/Counter
  - 1xRTC (real-time clock), supports leap year perpetual calendar, alarm event, periodic wake-up, supports internal and external clock calibration
  - 2x16 bit Advanced Timer Counters, supports input capture, complementary output, quadrature encoding input, 4 independent channels, of which 3 channels support 6 complementary PWM outputs
  - 1x16 bit General Timer, 4 independent channels, supports input capture/output comparison/PWM output
  - 1x16 bit Basic Timer
  - 1 x 16 bit Low-Power Timer

  - 1 x 24 bit SysTick
  - 1x 7 bit Window Watchdog (WWDG)
  - 1x12 bit Independent Watchdog (IWDG)
- Hardware Divider (HDIV) and Square Root (SQRT)
- Security features
- Flash storage encryption
- CRC16/32 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports clock failure monitoring, anti-dismantling monitoring
- 96-bit UID and 128-bit UCID

RF Features

- Working frequency： 113 - 960 MHz
- Modulation style: 2 (G)FSK, 4 (G)FSK, OOK
- Data rate： 0.1 - 1000 kbps
- Sensitivity： 2 FSK, -122 dBm DR=2.4 kbps, 433.92 MHz
  4 FSK, -88 dBm DR=1 Mbps,433.92 MHz
  OOK, -94 dBm DR= 300 kbps, 433.92 MHz
- RX current： 9.6 mA (DCDC) @ 433.92 MHz，FSK
  (Only apply for the RF operation current)
- TX current： 30 mA @ 13 dBm, 433.92 MHz, FSK / 82 mA@ 20 dBm,433.92 MHz, FSK
  (Only apply for the RF operation current)
- Supporting both direct and packet modes, with configurable packet handler and 128-Byte FIFO

System Features

- Working voltage： 1.8 – 3.6 V
- Working temperature： - 40 – 85 ℃
- Package: QFN 48 6x6

Overview

CMT2390F64 is an ultra-low power, high-performance, OOK / 2 (G)FSK / 4 (G)FSK based RF transceiver, applicable to various applications within the 113 - 960 MHz frequency band. The product is part of the CMOSTEK NextGenRF™ product family which covers a complete product line consisting of transmitters, receivers and transceivers. The high-density integration of CMT2390F64 simplifies the required BOM in system design. With Tx power reaching +20 dBm and sensitivity reaching -122 dBm, it can achieve optimized performance of application RF links. Through providing multiple data packet formats and code methods, this product ensures the flexible supporting of various applications. Besides, the CMT2390F64 provides functions such as 128-byte Tx/Rx FIFO, multiple GPIO and interrupt configurations, Duty-Cycle mode, LBT (listen before talk), high-precision RSSI, LBD, power on reset, low-frequency clock output, quick frequency hopping, squelch, etc., which allows more flexible application design and gains more product differentiation capability.

Application

- Auto metering
- Home security and building automation
- Wireless sensor nodes and industrial monitoring
- ISM band data communication
- Tag reader and writer

Table1. CMT2390F64 Resources List

Memory		Analog peripheral		Digital peripheral								Package
ROM	RAM	ADC	PDR	RTC	WDT	Timer	UART	SPI	I2C	I2S	GPIO	
64 KB Flash	8 KB	12 bits x 6-ch 1Msps	√	1	2	5	2xUSART 1xLPUART	2	2	1	23	QFN48

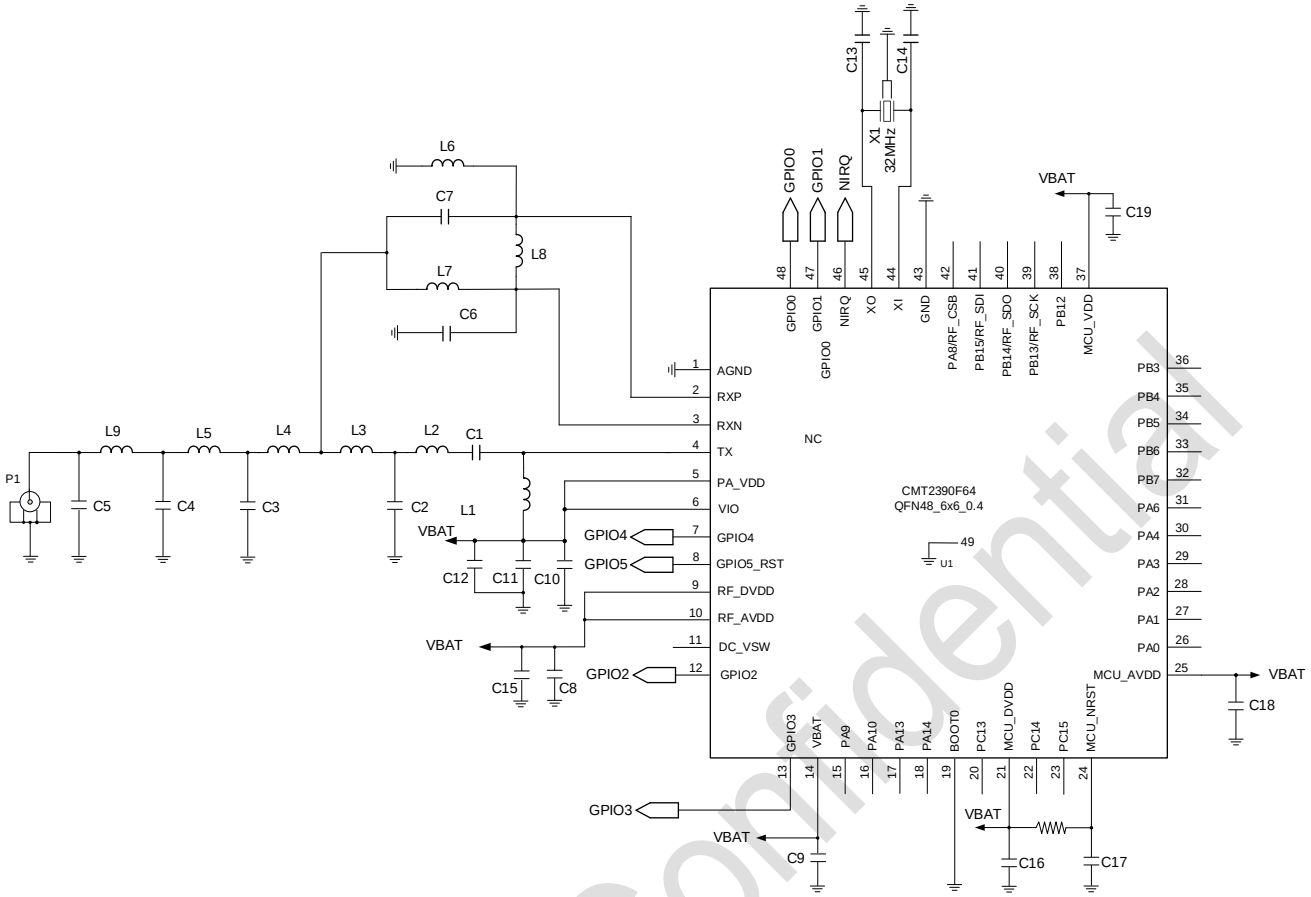


Figure 1-1. CMT2390F64 (QFN 48 6x6) Typical Application Diagram (disable DC-DC)

Table 1-1. BOM of 20 dBm Direct Tie (disable DC-DC)

Signa	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	22	12	12	12	pF	
C2	±5%, 0402 NP0, 50 V	6.8	5.6	3.3	3.3	pF	
C3	±5%, 0402 NP0, 50 V	8.2	6.2	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	8.2	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
C15	±5%, 0402 NP0, 50 V	100				nF	
C16	±5%, 0402 NP0, 50 V	100				nF	
C17	±5%, 0402 NP0, 50 V	100				nF	
C18	±5%, 0402 NP0, 50 V	100				nF	
C19	±5%, 0402 NP0, 50 V	100				nF	
L1	±5%, 0603 Ceramic Chip Inductor	220	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Ceramic Chip Inductor	68	47	15	12	nH	Sunlord SDCL

Signa	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
L3	±5%, 0603 Ceramic Chip Inductor	56	39	15	12	nH	Sunlord SDCL
L4	±5%, 0603 Ceramic Chip Inductor	33	33	8.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Ceramic Chip Inductor	47	33	8.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Ceramic Chip Inductor	220	68	33	33	nH	Sunlord SDCL
L9	±5%, 0603 Ceramic Chip Inductor	33	NC	NC	NC	nH	Sunlord SDCL
R1	±10%, 0603 Ceramic Chip Resistance	10k				Ω	
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2390F64 RF Receiver and Transmitter					-	CMOSTEK

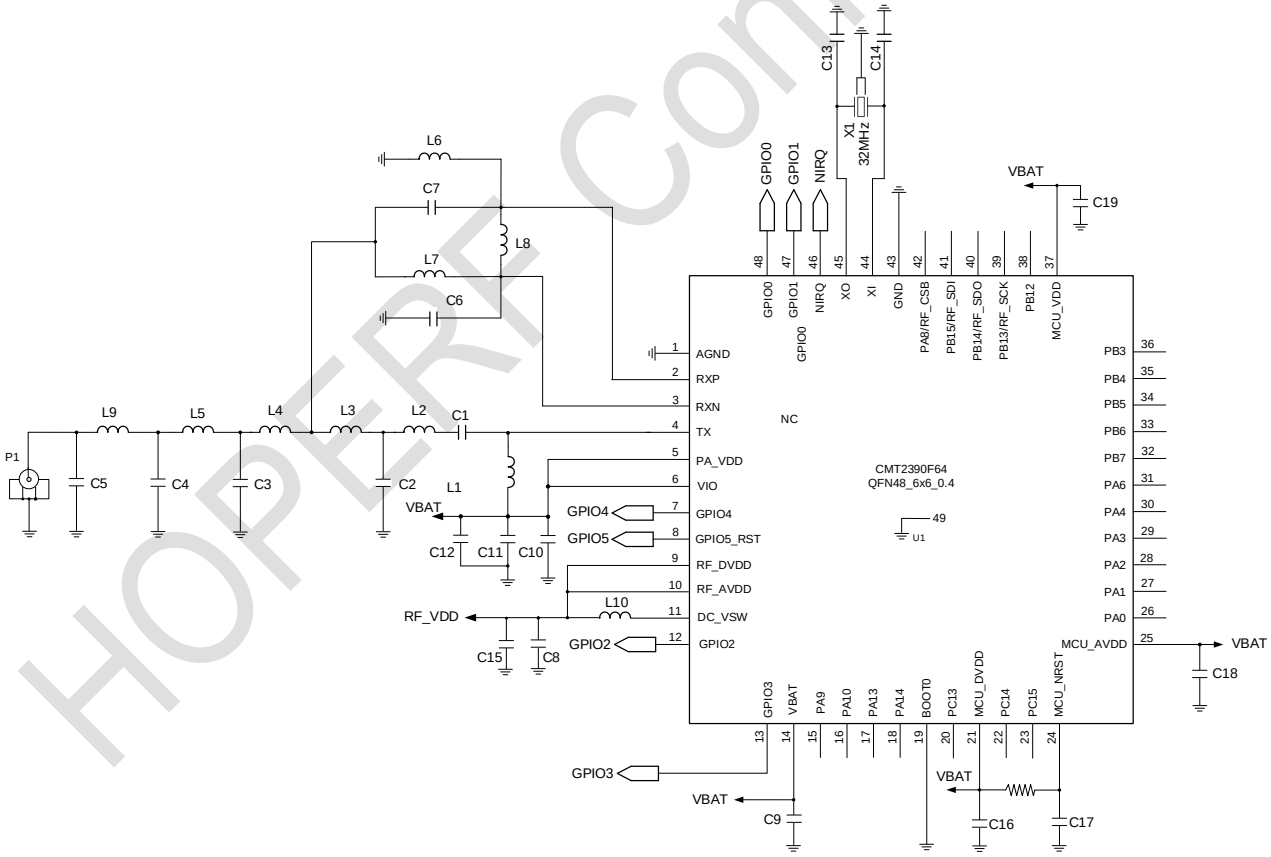


Figure 1-2. CMT2390F64 (QFN 48 6x6) Typical Application Diagram (enable DC-DC)

Table 1-2. BOM of 20 dBm Direct Tie (enable DC-DC)

Signal	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	22	12	12	12	pF	
C2	±5%, 0402 NP0, 50 V	6.8	5.6	3.3	3.3	pF	
C3	±5%, 0402 NP0, 50 V	8.2	6.2	3.3	3.0	pF	
C4	±5%, 0402 NP0, 50 V	8.2	NC	NC	NC	pF	
C5	±5%, 0402 NP0, 50 V	NC	NC	NC	NC	pF	
C6	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C7	±5%, 0402 NP0, 50 V	5.6	3.9	1.8	1.8	pF	
C8	±5%, 0603 NP0, 50 V	2.2				uF	
C9	±5%, 0402 NP0, 50 V	1				uF	
C10	±5%, 0402 NP0, 50 V	220				pF	
C11	±5%, 0402 NP0, 50 V	100				nF	
C12	±5%, 0603 NP0, 50 V	4.7				uF	
C13	±5%, 0402 NP0, 50 V	NC				pF	
C14	±5%, 0402 NP0, 50 V	NC				pF	
C15	±5%, 0402 NP0, 50 V	100				nF	
C16	±5%, 0402 NP0, 50 V	100				nF	
C17	±5%, 0402 NP0, 50 V	100				nF	
C18	±5%, 0402 NP0, 50 V	100				nF	
C19	±5%, 0402 NP0, 50 V	100				nF	
L1	±5%, 0603 Ceramic Chip Inductor	220	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Ceramic Chip Inductor	68	47	15	12	nH	Sunlord SDCL
L3	±5%, 0603 Ceramic Chip Inductor	56	39	15	12	nH	Sunlord SDCL
L4	±5%, 0603 Ceramic Chip Inductor	33	33	8.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Ceramic Chip Inductor	47	33	8.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Ceramic Chip Inductor	47	33	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Ceramic Chip Inductor	220	68	33	33	nH	Sunlord SDCL
L9	±5%, 0603 Ceramic Chip Inductor	33	NC	NC	NC	nH	Sunlord SDCL
L10	MPH252012C100MT, 10UH ±20%, package 2520, DC resistance 0.5Ω, saturation current 0.5A	10				uH	Sunlord

Signal	Description	Component Value				Unit	Supplier
		315 MHz +20 dBm	433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
R1	±10%, 0603 Ceramic Chip Resistance	10k				Ω	
X1	±10 ppm, SMD	32				MHz	EPSON
U1	CMT2390F64 RF Receiver and Transmitter					-	CMOSTEK

Table of Contents

1 Electrical Characteristic

VDD= 3.3 V，TOP= 25 °C，FRF = 433.92 MHz, sensitivity is measured by receiving a PN9 coded data and matching impedance to 50Ω under 0.1% BER standard.Unless otherwise stated, all results are tested on the CMT2390F64-EM evaluation board.

1.1 Recommended Operation Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		- 40		85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Rating

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	V_{DD}		- 0.3	3.6	V
Interface voltage	V_{IN}		- 0.3	3.6	V
Junction temperature	T_J		- 40	125	℃
Storage temperature	T_{STG}		- 50	150	℃
Soldering temperature	T_{SDR}	Last for at least 30 seconds Human body model (HBM)		255	℃
ESD rating[2]		Human body model (HBM)	- 2	2	kV
Latch-up current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2390F64 is a high-performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Parameter	Symbol	Condition		Typ. (Disable DCDC)	Typ. (Enable DCDC)	Unit
Sleep current [1]	I_{SLEEP}	In sleep mode with sleep timer disabled		400		nA
		In sleep mode with sleep timer enabled		800		nA
Ready current [1]	I_{Ready}			2.1	1.9	mA
RFS current [1]	I_{RFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
TFS current [1]	I_{TFS}		315 MHz	7.5	5.2	mA
			433 MHz	7.8	5.6	mA
			868 MHz	8.4	5.9	mA
			915 MHz	8.5	5.9	mA
RX current [1]	I_{Rx}	DR = 10 kbps Dev =10 kHz	315 MHz	13.5	8.8	mA
			433 MHz	13.6	9.4	mA
			868 MHz	14.3	9.9	mA
			915 MHz	14.3	9.9	mA
TX current [1]	I_{Tx}	20 dBm[2]	315 MHz	74	/	mA
			433 MHz	82	81	mA
			868 MHz	88	87	mA
			915 MHz	88	87	mA
		13 dBm [3]	315 MHz	26.7	/	mA
			433 MHz	30	29	mA
			868 MHz	33	32	mA
			915 MHz	34	33	mA
		10 dBm [3]	315 MHz	21	15	mA
			433 MHz	25	24	mA
			868 MHz	27	26	mA
			915 MHz	27	26	mA
		-10 dBm [3]	315 MHz	10.3	7	mA
			433 MHz	11	10	mA
			868 MHz	12	11	mA
			915 MHz	12	11	mA

Notes:

[1]. 2 FSK, DR = 10 kbps, FDEV = 5 kHz, Vbat = 3.3 V.

[2]. Apply 20 dBm matching network.

[3]. Apply 13 dBm matching network.

[4]. Only apply for RF operating current, not included the MCU working current.

1.4 RF Receiver Specification

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Data rate	DR	OOK		0.1		300	kbps
		2 (G)FSK		0.1		500	kbps
		4 (GFSK		0.1		1000	kbps
Deviation (RX)	F_{DEV}	(G)FSK, 4 (G)FSK[1]		0.5		350	kHz
Sensitivity @ 433 MHz (direct tie matching network)	S_{433}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz, BW= 4.8 kHz		-122		dBm
			DR = 10 kbps, F_{DEV} = 5 kHz		-114		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-112		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
			DR = 100 kbps, F_{DEV} = 50 kHz		-106		dBm
			DR = 200 kbps, F_{DEV} = 100 kHz		-104		dBm
			DR = 500 kbps, F_{DEV} = 250 kHz		-98		dBm
		OOK[2]	5 kbps		-110		dBm
			50 kbps		-101		dBm
			100 kbps		-97		dBm
			200 kbps		-95		dBm
			300 kbps		-94		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10 kHz		-109		dBm
			DR = 100 kbps, F_{DEV}[3] =100 kHz		-99		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-88		dBm
Sensitivity @ 868 MHz (direct tie matching network)	S_{868}	FSK[2]	DR = 2.4 kbps, F_{DEV} = 1.2 kHz, BW = 4.8 kHz		-120		dBm
			DR = 10 kbps,F_{DEV} = 5 kHz		-111		dBm
			DR = 20 kbps, F_{DEV} = 10 kHz		-110		dBm
			DR = 50 kbps, F_{DEV} = 25 kHz		-107		dBm
			DR = 100 kbps, F_{DEV} = 50 kHz		-104		dBm
			DR = 200 kbps, F_{DEV} = 100 kHz		-102		dBm
			DR = 500 kbps, F_{DEV} = 250 kHz		-96		dBm
		OOK[2]	5 kbps		-106		dBm
			50 kbps		-98		dBm
			100 kbps		-94		dBm
			200 kbps		-93		dBm
			300 kbps		-92		dBm
		4FSK[2]	DR = 10 kbps, F_{DEV}[3] = 10 kHz		-106		dBm
			DR = 100 kbps, F_{DEV}[3] = 100 kHz		-96		dBm
			DR = 1 Mbps, F_{DEV}[3] = 250 kHz		-85		dBm
Notes: [1]. BT = 0.5 by default for Gaussian modulation. [2]. In case of unspecified BW value, a crystal of 10 ppm is used and the BW value is automatically calculated by RFPDK. [3]. For 4 FSK, FDEV represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.							
Receiver channel bandwidth	BW	Receiver channel bandwidth		1.3		1168	kHz
Saturation input signal level	P_{LVL}					20	dBm

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
RSSI range	RSSI	By one step of 1 dB		-127		20	dBm
Co-channel rejection @ 433 MHz，868 MHz	CCR	DR = 2.4 kbps; FDEV = 1.2 kHz; BW = 4.8 kHz CW interference, BER<0.1%			-7		dBc
Adjacent channel rejection @ 433 MHz	ACR-I_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER<0.1%			62		dBc
Adjacent channel rejection @ 868 MHz	ACR-I_{868}	DR = 2.4 kbps；F_{DEV} = 1.2 kHz; BW = 4.8 kHz, Channel Space = 12.5 kHz， CW interference, BER < 0.1%			56		dBc
Blocking @ 433 MHz	BI_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, CW interference, BER < 0.1%	±1 MHz offset		76		dBc
			±2 MHz offset		80		dBc
			±10 MHz offset		84		dBc
Blocking @ 868 MHz	BI_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz, CW interference, BER < 0.1%	±1 MHz offset		66		dBc
			±2 MHz offset		76		dBc
			±10 MHz offset		83		dBc
Image Rejection @ 433 MHz	IMR_{433}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz CW interference, BER < 0.1%	Before calibration		30		dBc
			After calibration		56		dBc
Image Rejection @ 868 MHz	IMR_{868}	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; BW = 4.8 kHz CW interference, BER < 0.1%	Before calibration		26		dBc
			After calibration		51		dBc
Input 3rd order intercept point @ 433 MHz	$IIP3_{433}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-13		dBm
Input 3rd order intercept point @ 868 MHz	$IIP3_{868}$	DR = 2.4 kbps; F_{DEV} = 1.2 kHz; two-tone test with 10 MHz and 20 MHz deviations.			-12		dBm
Receiver input impedance	Zin	RXP and RXN Differential input impedance	433 MHz	150 Ω// 0.8 pF			
			868 MHz	134 Ω// 1.0 pF			

1.5 RF Transmitter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Specific peripheral components are required according to different frequency bands.	-10		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power change in different temperature	$P_{OUT-TOP}$	Temperature range: -40 to +85 °C		1		dB
Spurious emissions		P_{OUT} = +13 dBm, 433 MHz, F_{RF} < 1 GHz			-54	dBm
		1 GHz to 12.75 GHz, including Harmonic			-36	dBm
Harmonic output[1] for FRF= 315 MHz	$H2_{315}$	2nd harmonic, +20 dBm P_{OUT}		-57		dBm
	$H3_{315}$	3rd harmonic, +20 dBm P_{OUT}		-75		dBm
Harmonic output[1] for FRF= 433 MHz	$H2_{433}$	2nd harmonic, +20 dBm P_{OUT}		-56		dBm
	$H3_{433}$	3rd harmonic, +20 dBm P_{OUT}		-71		dBm
Harmonic output[1] for FRF= 868 MHz	$H2_{868}$	2nd harmonic, +20 dBm P_{OUT}		-47		dBm
	$H3_{868}$	3rd harmonic, +20 dBm P_{OUT}		-72		dBm
Harmonic output[1] for FRF= 915 MHz	$H2_{915}$	2nd harmonic, +20 dBm P_{OUT}		-47		dBm
	$H3_{915}$	3rd harmonic, +20 dBm P_{OUT}		-73		dBm
Harmonic output[1] for FRF= 315 MHz	$H2_{315}$	2nd harmonic, +13 dBm P_{OUT}		-51		dBm
	$H3_{315}$	3rd harmonic, +13 dBm P_{OUT}		-72		dBm
Harmonic output[1] for FRF= 433 MHz	$H2_{433}$	2nd harmonic, +13 dBm P_{OUT}		-44		dBm
	$H3_{433}$	3rd harmonic, +13 dBm P_{OUT}		-58		dBm
Harmonic output[1] for FRF= 868 MHz	$H2_{868}$	2nd harmonic, +13 dBm P_{OUT}		-50		dBm
	$H3_{868}$	3rd harmonic, +13 dBm P_{OUT}		-71		dBm
Harmonic output[1] for FRF= 915 MHz	$H2_{915}$	2nd harmonic, +13 dBm P_{OUT}		-54		dBm
	$H3_{915}$	3rd harmonic, +13 dBm P_{OUT}		-73		dBm

Notes:

[1]. The harmonic level mainly depends on the quality of matching network. The parameters above are measured on CMT2390F64-EM.

1.6 Settling Time of RF Status Switching

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settling time	T_{SLP-RX}	From Sleep to RX		660		us
	T_{SLP-TX}	From Sleep to TX		660		us
	T_{STB-RX}	From Standby to RX		160		us
	T_{STB-TX}	From Standby to TX		160		us
	T_{RFS-RX}	From RFS to RX		16		us
	T_{TFS-RX}	From TFS to TX		16		us
	T_{TX-RX}	From TX to RX (Ramp down requires $2T_{symbol}$ time)		$2T_{symbol}$ +168		us
	T_{RX-TX}	From RX to TX		220		us

Notes:

[1]. T_{SLP-RX} and T_{SLP-TX} mainly depend on crystal oscillating, which is largely related to crystal itself.

1.7 RF Frequency Synthesizer

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Require different matching networks.	675		960	MHz
			338		640	MHz
			113		320	MHz
Frequency deviation range	F_{DEV_RNG} [1]	675 ~ 960 MHz		600		kHz
		450 ~ 640 MHz		400		kHz
		338 ~ 450 MHz		300		kHz
		225 ~ 320 MHz		200		kHz
		169 ~ 225 MHz		150		kHz
		135 ~ 169 MHz		120		kHz
		113 ~ 135 MHz		100		kHz
Frequency resolution	F_{RES}			60		Hz
Frequency tuning time	t_{TUNE}			60		us
Phase noise @ 433 MHz	PN_{433}	10 kHz Frequency Offset		-101		dBc/Hz
		100 kHz Frequency Offset		-114		dBc/Hz
		1 MHz Frequency Offset		-129		dBc/Hz
		10 MHz Frequency Offset		-134		dBc/Hz
Phase noise @ 868 MHz	PN_{868}	10 kHz Frequency Offset		-100		dBc/Hz
		100 kHz Frequency Offset		-109		dBc/Hz
		1 MHz Frequency Offset		-126		dBc/Hz
		10 MHz Frequency Offset		-129		dBc/Hz

Notes:

[1]. For 2 FSK and 4 FSK, F_{DEV} represents the frequency difference between the frequency points at the far ends (left and right) and the centered frequency point.

1.8 Crystal Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency [1]	F_{XTAL}			32		MHz
Crystal frequency precision [2]	$ppm_{\_XTAL}$		0	20	100	ppm
Load resistance	C_{LOAD_XTAL}			15		pF
Crystal equivalent resistance	Rm_{XTAL}			60		Ω
Crystal startup time [3]	t_{XTAL}			200		us

Notes:

[1]. The CMT2390F64 can utilize external reference clock to directly drive XIN pin through the coupling capacitor. The peak-to-peak value of external clock signal is required between 0.3 and 0.7 V.

[2]. It involves: (1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is largely related to crystal.

1.9 Controller Reset and Power Control Module Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Rising	V_{PVD}	PLS[3:0]=0	1.8	1.88	1.96	V
Falling		PLS[3:0]=0	1.7	1.78	1.86	
Rising		PLS[3:0]=1	2	2.08	2.16	
Falling		PLS[3:0]=1	1.9	1.98	2.06	
Rising		PLS[3:0]=2	2.2	2.28	2.36	
Falling		PLS[3:0]=2	2.1	2.18	2.26	
Rising		PLS[3:0]=3	2.4	2.48	2.56	
Falling		PLS[3:0]=3	2.3	2.38	2.46	
Rising		PLS[3:0]=4	2.6	2.68	2.76	
Falling		PLS[3:0]=4	2.5	2.58	2.66	
Rising		PLS[3:0]=5	2.8	2.88	2.96	
Falling		PLS[3:0]=5	2.7	2.78	2.86	
Rising		PLS[3:0]=6	3	3.08	3.16	
Falling		PLS[3:0]=6	2.9	2.98	3.06	
Rising		PLS[3:0]=7	3.2	3.28	3.36	
Falling		PLS[3:0]=7	3.1	3.18	3.26	
Rising		PLS[3:0]=8	3.4	3.48	3.56	
Falling		PLS[3:0]=8	3.3	3.38	3.46	
Rising		PLS[3:0]=9	3.6	3.68	3.76	
Falling		PLS[3:0]=9	3.5	3.58	3.66	
Rising		PLS[3:0]=10	3.8	3.88	3.96	
Falling		PLS[3:0]=10	3.7	3.78	3.86	
PVD delay	$V_{PVDhyst}$(2)	-	80	100	125	mV
VDD Power up/down Reset Threshold	V_{POR}	-	-	1.53	-	V

1.10 Controller Embedded Reference Voltage

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Embedded Reference Voltage	V_{REFINT}	- 40℃ < TA < +105℃	1.16	1.21	1.26	V
Sampling time of ADC when internal reference voltage read out	$T_{S\_vrefint}$(1)	PLS [2:0]=001 (rising edge)	-	10	-	μs
1. The minimum sampling time was obtained from multiple cycles in application.						

1.11 Controller Working Current Characteristic

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin turnover rate, program location in memory, and code executed, etc.

- **Maximum current consumption**

The micro-controller is in the following conditions：

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the fHCLK frequency (0 wait period for 0 to 18 MHz, 1 wait period for 18 to 36 MHz, 2 waiting period for over 36 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on： $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

Table 1-11. Maximum Current Consumption in Operating Mode When Data Processing Code Runs in ROM

Parameter	Sign	Condition	f_{HCLK}	Typical Value (1)	Unit
Operating current in the operating mode	I_{DD}	External clock(2)，enable all the peripherals	48 MHz	8.4	mA
			24 MHz	5.0	
			8 MHz	2.8	
		External clock(2)，disable all the peripherals	48 MHz	5.0	
			24 MHz	3.3	
			8 MHz	2.3	
1. Guaranteed by design and comprehensive assessment, not tested in production. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Table 1-12. Maximum Current Consumption in Operating Mode When Data Processing Code Runs in Internal RAM

Parameter	Symbol	Condition	f_{HCLK}	Typ. (1)	Unit
Operating current in the operating mode	I_{DD}	External clock(2)，enable all the peripherals	48 MHz	6.2	mA
			24 MHz	4.1	
			8 MHz	3.2	
		External clock(2)，disable all the peripherals	48 MHz	4.4	
			24 MHz	3.2	
			8 MHz	2.6	
1. Guaranteed by design and comprehensive assessment, not tested in production. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Table 1-13. Maximum Current Consumption in Sleep Mode when Data Processing Code Runs in Internal Flash Memory

Parameter	Symbol	Condition	f_{HCLK}	Typ. (1)	Unit
Working current in sleep mode	I_{DD}	External clock(2)，enable all the peripherals	48 MHz	6.5	mA
			24 MHz	3.9	
			8 MHz	2.0	
		External clock(2)，disable all the peripherals	48 MHz	2.9	
			24 MHz	2.1	
			8 MHz	1.4	
1. According to the comprehensive assessment, V_{DDmax} and $f_{HCLKmax}$ enabling peripherals are the test condition. 2. External clock, PLL is enabled when the f_{HCLK} is 24 MHz or 48 MHz.					

Table 1-14. Typical Consumption in Stop and Sleep Mode

Parameter	Symbol	Condition	Typ(1)	Max	Unit
			V_{DD}=3.3V	V_{DD}=3.3V	
SLEEP mode current		Kernel stopped, all peripherals including Cortex-M 0 core peripherals such as NVIC, system ticking clock (SysTick) still running	2.7	5	mA
STOP mode current		RTC is disabled, SRAM, registers and all I/O states retain	1.5	2.5	uA
PD mode current		VDD power down mode, 3 WAKEUP IO and NRST can be awakened	0.5	1	uA
1. Typ/ Max value is tested under TA=25 ℃.					

- **Typical current consumption**

MCU is under the following conditions：

- All I / O pins are in input mode and are connected to a static level VDD or VSS with no load.
- All peripherals are disabled, unless otherwise noted.
- The access time of the flash memory is adjusted to the fHCLK frequency (0 wait period for 0 to 18 MHz, 1 wait period for 18 to 36 MHz, 2 waiting period for over 36 MHz).
- The command pre-fetch function is turned on (notes: this parameter must be set before the clock and bus frequency distribution is set).
- When the peripherals are turned on：$f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/3$.

Table 1-15. Typical Current Consumption in Operation Mode When Data Processing Code Runs in Internal Flash

Parameter	Symbol	Condition	f_{HCLK}	Typ(1)		Unit
				Enable all the peripherals	Disable all the peripherals	
Supply current in operating mode	I_{DD}	External high speed clock (HSE,) using AHB prefrequency to reduce the frequency	48 MHz	8.2	4.8	mA
			24 MHz	5.0	3.3	
			8 MHz	2.7	2.1	
		Internal high speed RC oscillator (2) (HSI)，AHB pre-frequency to reduce the frequency	48 MHz	7.6	4.3	mA
			24 MHz	4.3	2.7	
			8 MHz	2.1	1.5	
1. Typical value is tested under TA=25℃, VDD=3.3 V. 2. The internal high-speed clock is 8 MHz，and PLL is enabled when f_{HCLK} >8 MHz.						

Table 1-16. Typical Current Consumption in Sleep Mode When Data Processing Code Runs in Internal Flash or RAM

Parameter	Symbol	Condition	f_{HCLK}	Typ(1)		Unit
				Enable all the peripherals	Disable all the peripherals	
Working current in sleep mode	I_{DD}	External high speed clock (HSE)，using AHB prefrequency to reduce the frequency	48 MHz	6.3	2.7	mA
			24 MHz	3.7	2.0	
			8 MHz	1.8	1.2	
		Internal high speed RC oscillator(2) (HSI)， AHB pre-frequency to reduce the frequency	48 MHz	5.7	2.1	mA
			24 MHz	3.1	1.4	
			8 MHz	1.2	0.6	

1. Typical value is tested under TA=25 ℃, VDD=3.3 V.
2. The internal high-speed clock is 8 MHz，and PLL is enabled when fHCLK > 8 MHz.

1.12 External Clock Source Charateristic

- High-speed external user clock generated from external oscillation sources

  The characteristic parameters in the following table are measured under a high-speed external clock source and the ambient temperature and supply voltage meet the conditions in the following table.

Table 1-17. High-speed External User Clock Features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency	-	4	8	20	MHz
V_{HSEH}	OSC_IN input pin at high-level voltage(1)		0.7	-		V
V_{HSEL}	OSC_IN input pin at low-level voltage(1)			-	0.3	
$t_{w(HSE)}$	OSC_IN high /low time(1)		16	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC_IN up/ down time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance (1)			5		pF
$DuCy_{(HSE)}$	Duty cycle(1)		45	-	55	%
I_L	OSC_IN input leakage current(1)	VSS≤VIN≤VDD	-	-	±1	μA

1.Guaranteed by design and comprehensive evaluation, not tested in production.

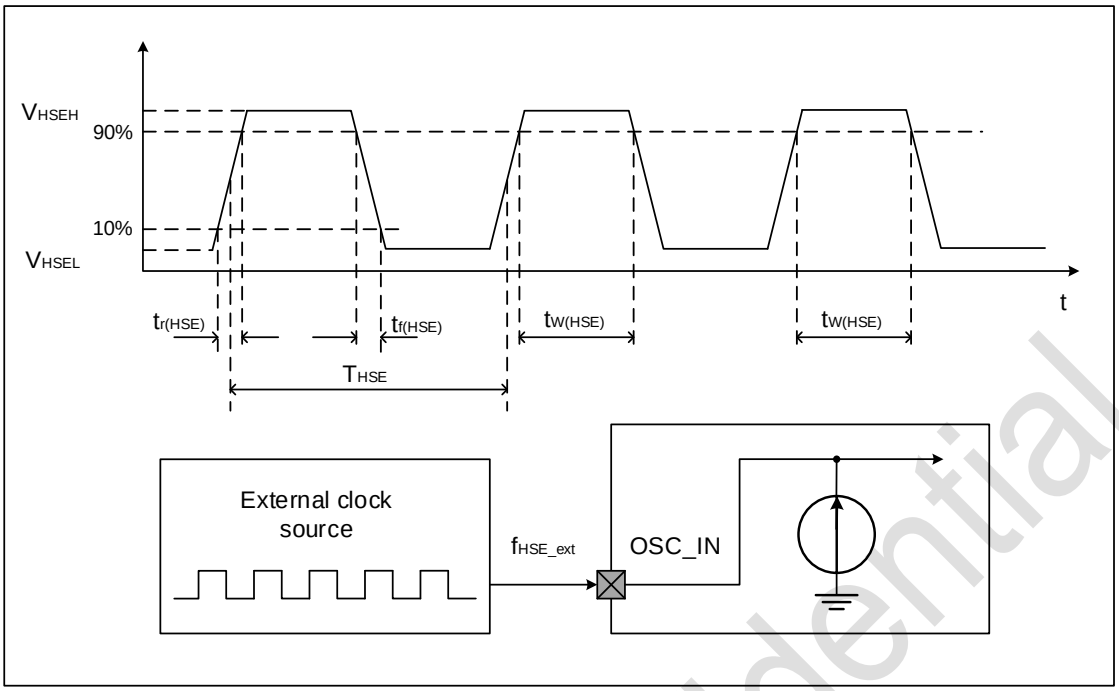


Figure 1-3. The AC Timing Diagram of External High-speed Clock Source

- **Low-speed external user clock generated from external oscillation sources**

Table 1-18. Low-speed External User Clock Features

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin at high-level voltage(1)		0.7	-		V
V_{LSEL}	OSC32_IN input pin at low-level voltage(1)			-	0.3	
$tw_{(LSE)}$	OSC32_IN high /low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN up/ down time(1)		-	-	10	
$DuCy_{(LSE)}$	Duty cycle(1)		30	-	70	%
I_L	OSC32_IN input leakage current(1)	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA
1. Guaranteed by design and comprehensive assessment, not tested in production。						

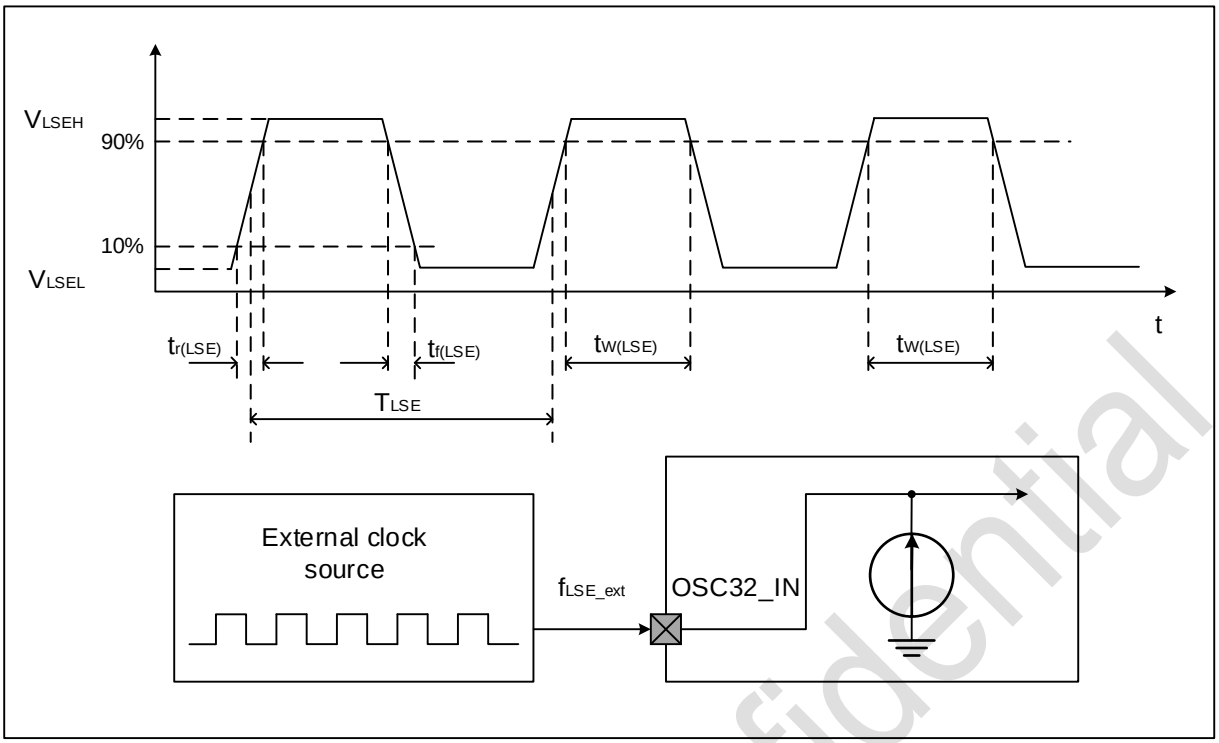


Figure 1-4. AC Timing Diagram of the External Low-speed Clock Source

- **A high-speed external clock generated by using crystal / ceramic resonator**

The high speed external clock (HSE) can be generated using an oscillator consisting of a 4～20 MHz crystal/ceramic oscillator. The information given in this section is based on the use of typical external components listed in the table below. In applications where the oscillator and load capacitance must be as close to the oscillator pin as possible to reduce output distortion and stability time at startup. For detailed parameters of crystal oscillator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer (the crystal resonators mentioned here are usually referred to the passive crystal oscillator).

Table 1-19. HSE 4～20 MHz Oscillator Characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	20	MHz
C_{L1} C_{L2}(3)	The suggested load capacitance and corresponding crystal serial resistance（R_S）	R_S = 30 Ω	-	20	--	pF
i_2	HSE drive current	V_{DD} = 3.3 V, V_{IN} = V_{SS} 30pF load	-	1.1	1.6	mA
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stable		3		ms

1. The parameters of the resonator are given by the crystal resonator manufacturer.
2. Guaranteed by design and comprehensive assessment, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric capacitance (typically) between 5pF and 25pF designed for high-frequency applications, and to select suitable crystals or resonators. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}. The capacitive reactance of PCB and MCU pins should be taken into account when selecting C_{L1} and C_{L2}.
4. tSU(HSE) is the startup time. It is measured from the time when HSE is enabled by software until a stable 8 MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

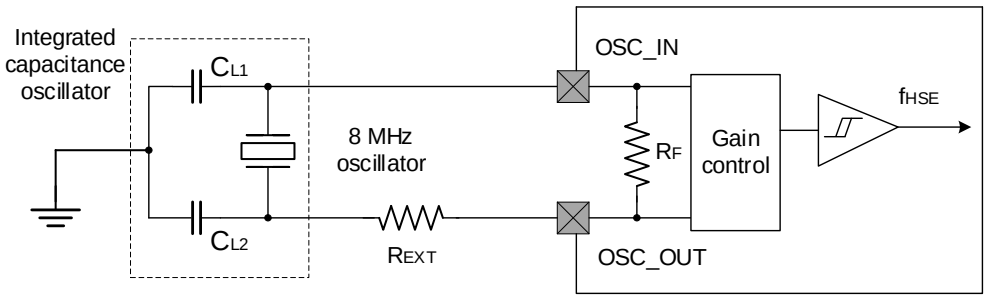


Figure 1-5. Typical Applications of 8 MHz Crystals

Note: The value of REXT is depended on the crystal characteristic.

- **A low-speed external clock generated by using a crystal / ceramic resonator**

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic oscillator. The information given in this section is based on the use of typical external components listed in the table below. In applications where the oscillator and load capacitance must be as close to the oscillator pin as possible to reduce output distortion and stability time at startup. For detailed parameters of crystal oscillator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer (the crystal resonators mentioned here are usually referred to the passive crystal oscillator).

Note: For CL1 and CL2, high quality porcelain dielectric capacitors between 5 p F and 15 p F and well-compliant crystals or oscillators are recommended. Usually, CL1 and CL2 have the same parameters. Crystal manufacturers usually give the parameters of the load capacitance as a serial combination of CL1 and CL2.
Load capacitance CL is calculated by the following equation: CL = CL1 CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitor of the pin and the capacitor associated with the PCB board or PCB.

Table 1-20. LSE Oscillator Characteristic (fLSE = 32.768 kHz)(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{L1} C_{L2}(2)	Recommended load capacitance and corresponding crystal serial impedance (RS)(3)	RS: 30 KΩ ~ 65 KΩ	-	-	20	pF
I2	LSE drive current	VDD = 3.3 V CL1 = CL2 = 12.5 pF RS = 30 KΩ	-	0.3	-	μA
$t_{SU(LSE)}$(4)	Startup time	VDD is stable	-	2	-	s

1. Guaranteed by design and comprehensive assessment, not tested in production.
2. See the attention and warning paragraph above this table.
3. Choose high quality oscillator with a small RS value that can optimize current consumption. Check with the crystal manufacturer for more details.
4. $t_{SU(LSE)}$ is the start time, measured from the software enabling LSE, until the stable 32.768 KHz oscillation is stabled.This value is measured on a standard crystal oscillator, which may vary greatly by the crystal manufacturer.

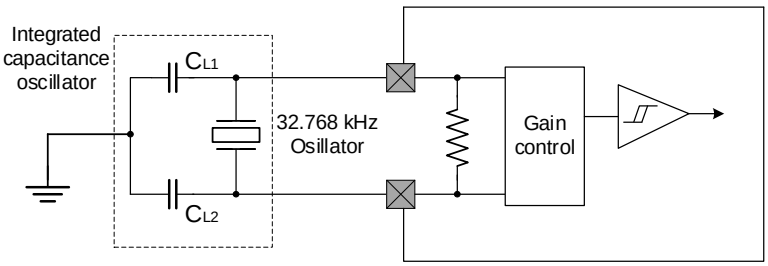


Figure 1-6. Typical Applications of Using 32.768 kHz Crystals

1.13 Controller Internal Clock Source Characteristics

- **High speed internal (HSI) RC Oscillator**

Table 1-21. HSI Oscillator Characteristic(1)(2)

Signal	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	Frequency	VDD=3.3 V，T_A= 25 ℃，after calibration	7.92	8	8.08	MHz
ACC_{HSI}	HSI oscillator temperature drift	VDD=3.3 V，T_A= - 40 ~ 105 ℃，temperature drift	-3	-	3	%
		VDD=3.3 V，T_A= - 10 ~ 85 ℃，temperature drift	-2.5	-	2	%
		VDD=3.3 V，T_A= 0 ~ 70 ℃，temperature drift	-2	-	1.5	%
$t_{SU(HSI)}$	HSI oscillator startup time		1	-	3	μs
$I_{DD(HSI)}$	HIS oscillator power consumption		-	80	150	μA

1. Unless otherwise specified, VDD = 3.3 V，TA = -40 ~ 85 ℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.

- **Low speed internal (LSI) RC oscillator**

Table 1-22. LSI Oscillator Characteristic(1)

Sign	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	output frequency	25℃ calibration, VDD = 3.3 V	29	30	31	KHz
		VDD = 1.8 V ~ 5.5 V, TA = -40 ~ 105 ℃	24	30	36	KHz
$t_{SU(LSI)}$ (3)	LSI oscillator start time		-	30	80	μs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption		-	0.2	-	μA

1. Unless otherwise specified, VDD = 3.3 V，TA = -40~85 ℃.
2. Guaranteed by design and comprehensive assessment, not tested in production.

1.14 Controller Low-power Mode Wake-up Time

The arousal time listed in the table below are measured during the arousal phase of an 8 MHz HIS RC oscillator. The clock source used on wake-up depends on the current mode of operation:

- Stop or Sleep mode：the clock source is RC oscillator
- Sleep mode：clock source is the clock used when entering into sleep mode

Table 1-23. Wake-up Time in Low-power Mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Awaken from sleep mode	16	HCLK(2)
t_{WUSTOP}(1)	Awaken from stop mode	20	us
t_{WUPD}(1)	Awaken from stanby mode	55	us

1. The awaken time counts from the beginning of the wakeup event until the user program reads the first instruction;
2. HCLK is the AHB clock frequency.

1.15 PLL Characteristics

Table 1-24. Internal PLL Characteristics

Symbol	Parameter	Num.			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock (2)	4	8	20	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	48	-	72	MHz
t_{LOCK}	PLL Ready indicates signal output time	-	-	50	μs
Jitter	TIE RMS Jitter	-	40	-	pS
Ipll	Operating Current of PLL @48 MHz VCO frequency.	-	300	500	uA

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. It is important to pay attention to the correct frequency multiplication factor, so that f_{PLL_OUT} is in the allowable range according to the PLL input clock frequency.

1.16 FLASH Characteristics

Table 1-25. FLASH Characteristics

Symbol	Parameter	Condition	Min(1)	Typ(1)	Max(1)	Unit
t_{prog}	Word programming time(32-bit)	TA = -40 ~ 85 ℃	-	175	-	μs
t_{ERASE}	Page erase time(512Bytes)	TA = -40 ~ 85 ℃	-	2.27	-	ms
t_{ME}	Mass erase time	TA = -40 ~ 85 ℃;	-	34.1	-	ms
I_{DD}	Supply current (1)	Read, f_{HCLK} = 48 MHz, VDD = 3.3 V	-	2	2.4	mA
		Write, f_{HCLK} = 48 MHz, VDD = 3.3 V	-	-	1.2	mA
		Erase, f_{HCLK} = 48 MHz, VDD = 3.3 V	-	-	0.6	mA
		PD mode, VDD = 3.3 ~ 3.6 V	-	-	150	μA

1. Guaranteed by design and comprehensive evaluation, not tested in production.

Table 1-26. Flash Memory Endurance and Data Retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance (Note: erasing and writing cycle)	TA = -40~85°C；	100	kcycles
t_{RET}	Data retention	TA = 85°C，after 1000 erasing cycle	10	years

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.17 I/O Port Characteristic

- Generic input/output characteristics

All of the I/O ports are compatible with CMOS and TTL.

Table 1-27. I/O Static Characteristics

Symbol	Parameter	VDD	Conditions	Min	Max	Unit
VIH	Low level input voltage	3.3	-	-	0.8	V
		1.8	-	-	0.2×VDD	
VIH	High level input voltage	3.3	-	2.0	-	
		1.8	-	0.8×VDD	-	
Vhys	I/O Schmitt trigger voltage Hysteresis (1)	3.3/1.8	-	0. 1×VDD	---	V
Ilkg (2)	Input leakage current IIH	3.3/1.8	-	---	1	μA
	Input leakage current IIL	3.3/1.8	-	-1	-	
VOH	Output high level voltage	3.3	High driving Imin=8 mA low driving Imin=4 mA	2.4	-	V
		1.8	High driving Imin=4 mA low driving Imin=2 mA	VDD-0.45	-	
VOL	Output low level voltage	3.3	High driving Imin=8 mA low driving Imin=4 mA	-	0.45	
		1.8	High driving Imin=4 mA low driving Imin=2 mA	-	0.4	
RPU	Internal pull-up resistor	3.3/1.8	-	40	100	kΩ
RPD	Internal pull-down resistor	3.3/1.8	-	40	100	kΩ
CIO	I/O pin capacitance	3.3/1.8	-	-	10	pF

1. The hysteresis voltage of the Schmitt trigger switching level. Guaranteed by design and comprehensive evaluation, not tested in production.

2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take most of the strict CMOS process or TTL parameters into account.

- Input and output AC characteristics

The parameters and definition of I/O AC are shown as followed.

Table 1-28. I/O AC Characteristics

VDD	Condition			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
3.3V (2.7~3.6)	Low (DR=1)	Slow (SR=1)	25	4	5.5	11	6.6	10	20
			50	7.5	9.5	18	8.5	12	24
			100	15	17	32	13	16	31
		Fast (SR=0)	25	3.8	4.9	9.2	5.9	8.8	18
			50	7.3	8.8	16.2	7.8	10.8	21.2
			100	14.2	16.7	30.5	12	15	29
	High (DR=0)	Slow (SR=1)	25	2.4	3.7	7.2	5.5	8.5	17.1

VDD	Condition			Rise/Fall Time (ns)			Propagation Delay (ns)		
	Driving Strength	Slew Rate Control	$C_{Loading}$(pf)	Min	Typ	Max	Min	Typ	Max
			50	3.9	5.5	10.5	6.5	9.6	19.2
			100	7.3	9.3	17.2	8.4	12	23
		Fast (SR=0)	25	2	3.1	5.9	4.9	7.6	16
			50	3.7	4.9	9.5	5.8	8.7	18
			100	7.2	8.8	17	7.7	11	22
1.8V (1.62~1.98)	Low (DR=1)	Slow (SR=1)	25	8	12	22	14	23	44
			50	15	20	36	18	27	52
			100	29	36	65	26	36	66
		Fast (SR=0)	25	7.5	10.5	16.4	12.25	20	40
			50	14.5	18.5	33	16.5	24.2	47
			100	28	35	62	24	33	62
	High (DR=0)	Slow (SR=1)	25	4.6	8	15.4	12	20.2	40
			50	7.6	11.8	22	14	22.5	44
			100	11.5	19.5	36	17.5	26.7	52
		Fast (SR=0)	25	4	6.9	14	10.5	18	36
			50	7.3	11	20	12.3	20	40
			100	15	18.5	33	16	25	47

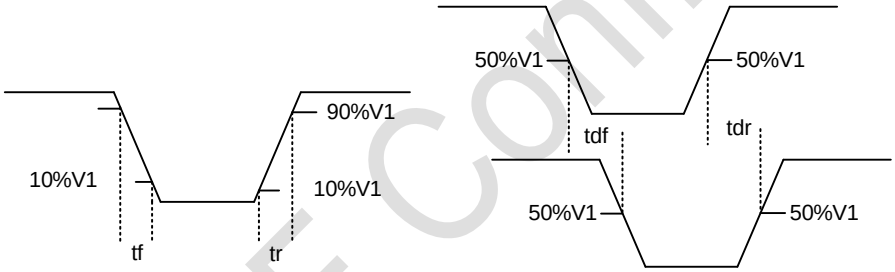


Figure1-7. I/O AC Characteristic Definition

1.18 MCU_NRST Pin Characteristics

NRST pin input driver uses CMOS technology. MCU_NRST pin is connected to a pull-up resistor that cannot be disconnected.

Table 1-29. NRST Pin Characteristics

Symbol	Parameter	VDD	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST low level input voltage	1.8 V ~ 3.6 V	-	-	0.3	V
$V_{IH(NRST)}$(1)	NRST high level input voltage	1.8 V ~ 3.6 V	0.7	-	-	
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis	1.8 V ~ 3.6 V	-	220	-	mV
R_{PU}	Internal pull-up resistor(2)	1.8 V ~ 3.6 V	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST input filter pulse	1.8 V ~ 2 V	-	-	100	ns
		3 V ~ 3.6 V	-	-	100	
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	1.8 V ~ 2 V	650	-	-	ns
		3 V ~ 3.6 V	300	-	-	

1. The reset network is to prevent parasitic reset.
2. Users must ensure that the potential of the NRST pin can be lower than the maximum VIL (NRST), otherwise the MCU cannot be reset.

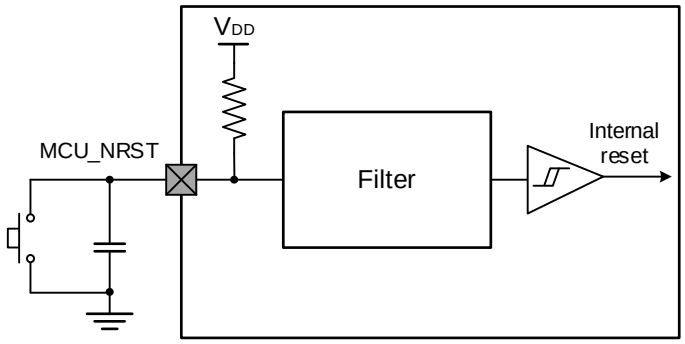


Figure 1-8. NRST Pin Protection Recommended Circuit Design

1.19 TIM Characteristic

Table 1-30. TIMx(1) Characteristic

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$= 48 MHz	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency from CH1 to CH2	$f_{TIMxCLK}$= 48 MHz	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	$f_{TIMxCLK}$= 48 MHz	-	16	bit
$t_{COUNTER}$	Select the internal clock, 16-bit counter clock cycle	$f_{TIMxCLK}$= 48 MHz	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	0.0208	1365	μs
t_{MAX_COUNT}	Maximum count	$f_{TIMxCLK}$= 48 MHz	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 48 MHz	-	89.478	s

1. TIMx is a common name and stands for TIM1~TIM8.

1.20 I2C Characteristic

The I2C interface complies with the standard I2C communication protocol while SDA and SCL are not "true" open-drain pins. When configured as open-drain output, the PMOS tube between the pin and VDD will be turned off, but still exists.

The I2C interface characteristic is shown as the following table.

Table 1-31. I²C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast + mode		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0	100	0	400	0	1000	KHz
$th_{(STA)}$	Start condition holding time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL Clock Low Time (1)	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time (1)	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Establishment time of repeated starting conditions (1)	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data retention time (1)	-	3.4	-	0.9	-	0.4	μs
$t_{su(SDA)}$	Establishment time of SDA (1)	250	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (1)	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (1)	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Establishment time of stop condition(1)	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle) (1)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacity load per bus (1)	-	400	-	400	-	200	pf
$t_{v(SDA)}$	Data validity time(1)	3.45	-	0.9	-	0.45	-	μs
$t_{v(ACK)}$	Response validity time (1)	3.45	-	0.9	-	0.45	-	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.

2. To achieve the maximum frequency of standard mode I2C, FPCLK1 must be greater than 2 MHz.To achieve the maximum frequency of fast mode I2C, FPCLK1 must behigher than 4 MHz.

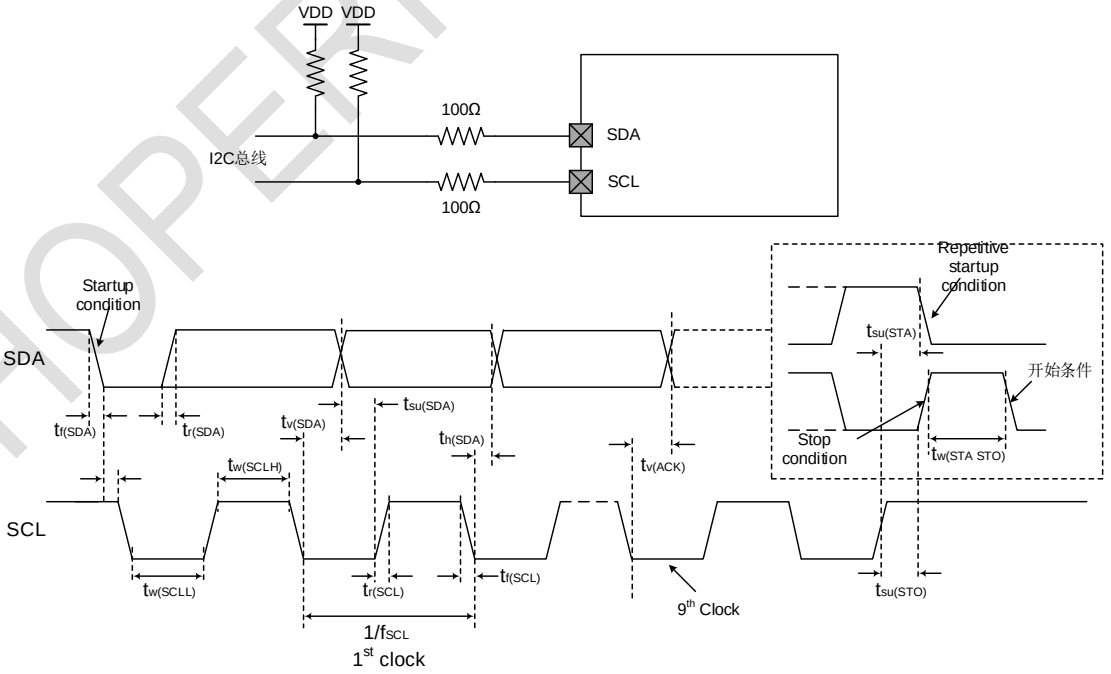


Figure 1-9. I²C Bus AC Waveform and Measurment Circuit (1)

1. The measuring point is set at CMOS level: 0.3 VDD and 0.7 VDD.

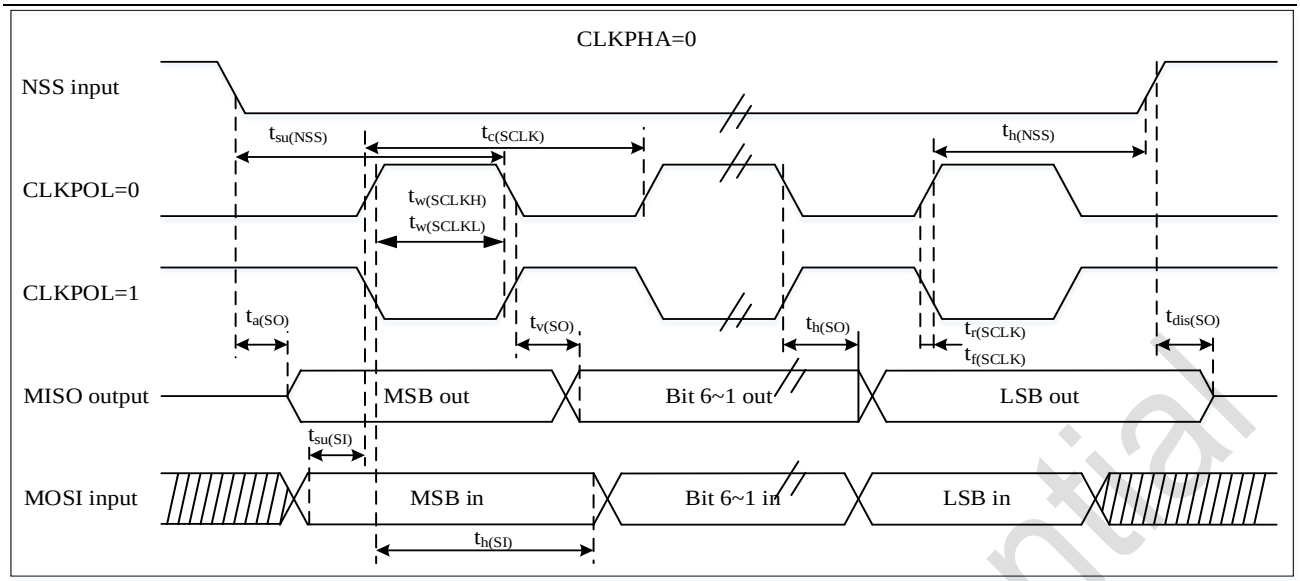
1.21 SPI/I2S Characteristic

For feature details of the input and output multiplexing pins (WS, CLK, SD of NSS, SCLK, SPI, MOSI, MISO, I2S), see Section 1.17.

Table 1-32. SPI Characteristics(4)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30 pF		-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave mode		30	70	%
$t_{su(NSS)}$(1)	NSS establishment time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS retention time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK}	t_{PCLK} + 2	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	SPI 1	19.84	-	ns
			SPI 2	20.5	-	
$t_{su(SI)}$(1)		Slave mode	SPI 1	4.16	-	
			SPI 2	4.16	-	
$t_{h(MI)}$(1)	Data input retention time	Master mode		0	-	ns
$t_{h(SI)}$(1)		Slave mode		4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode，f_{PCLK} = 20 MHz		0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(3)	Disabled time for data output	Slave mode		2	10	ns
$t_{v(SO)}$(1)	Valid time of data output	Slave mode (after the enabled edge)	SPI 1	-	32	ns
			SPI 2	-	30	
$t_{v(MO)}$(1)		Mastermode (after theenabled edge)	SPI 1	-	28	
			SPI 2	-	28	
$t_{h(SO)}$(1)	Data output retention time	Slave mode (after the enabled edge)		0	-	ns
$t_{h(MO)}$(1)		Master mode (after the enabled edge)		0	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The minimum value means the minimum time to drive the output, and the maximum value means the maximum time to get the data correctly.
3. The minimum value means the minimum time to turn off the output, and the maximum value means the maximum time to put the data line in the high resistance state.
4. Test voltage is 3.3 V.



Figire 1-10. SPI Sequence Diagram – Slave Mode and CPHA=0

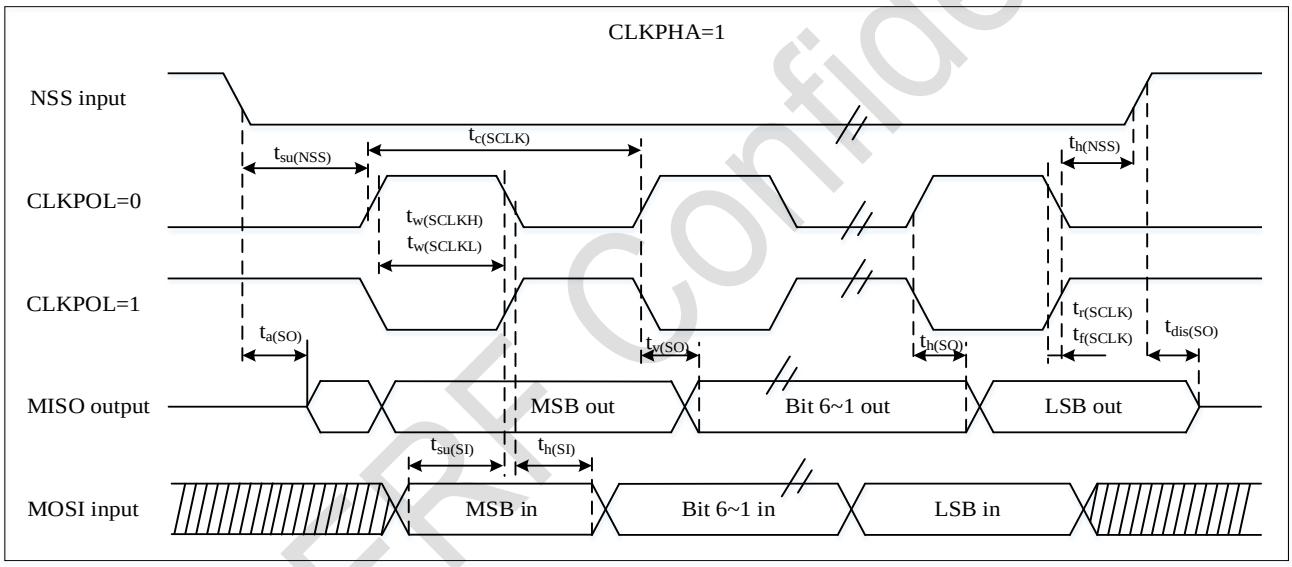


Figure 1-11. SPI Sequence Diagram - Slave Model and CPHA=1(1)

1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.

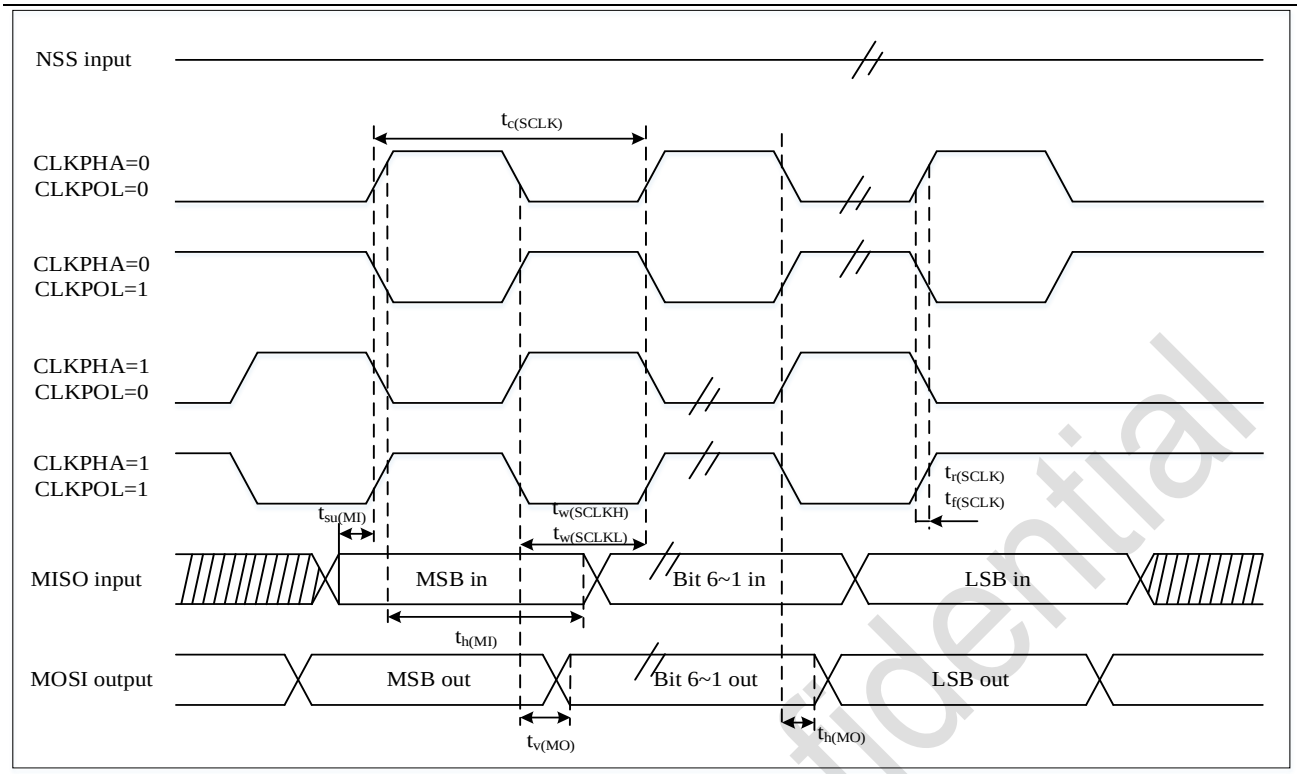


Figure 1-12. SPI Sequnece Diagram – Master Mode(1)

1. The measurement points are set at CMOS level: 0.3 VDD and 0.7 VDD.

Table 1-33. I²S Characteristic(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DuCy(SCK)	I2S from the input clock duty cycle	I2S Slave mode	30	50	70	%
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (16 bit)	-	2*Fs(3) *16	-	Hz
		Master mode (16 bit)	-	2*Fs(3) *16	-	
		Master mode (32 bit)	-	2*Fs(3) *32	-	
		Slave mode (32 bit)	-	2*Fs(3) *32	-	
$t_{r(CLK)}$	I2S clock up and down time	Load capacitance: CL = 50 pF	-	-	8	ns
$t_{v(WS)}$ (1)	WS validity time	Master mode	13.5	-	-	
$t_{h(WS)}$(1)	WS retention time	Master mode	0	-	-	
$t_{su(WS)}$(1)	WS establishment time	Slave mode	4	-	-	
$t_{h(WS)}$(1)	WS retention time	Slave mode	0	-	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, f_{PCLK} = 16 MHz, audio 48 kHz	312.5	-	-	
$t_{w(CLKL)}$(1)			345	-	-	
$t_{su(SD\_MR)}$(1)	Data entry setup time	master receiver	3.6	-	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	3.5	-	-	

$t_{h(SD\_MR)}$(1)(2)	Data entry retention time	master receiver	0	-	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0	-	-	
$t_{v(SD\_ST)}$(1)(2)	Valid time of data output	Slave transmitter (after the enabled edge)	-	-	29.76	ns
$t_{h(SD\_ST)}$(1)	Data output retention time	Slave generator (after the enabled edge)	0	-	-	
$t_{v(SD\_MT)}$(1)(2)	Valid time of data output	master generator (after the enabled edge)	-	-	13.6	
$t_{h(SD\_MT)}$(1)	Data output retention time	master generator (after the enabled edge)	-6.5	-	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. Relying on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then $T_{PCLK}=1/f_{PCLK}$=125 ns.
3. FS value audio sampling frequency, frequency range 8 KHz ~ 96 KHz.

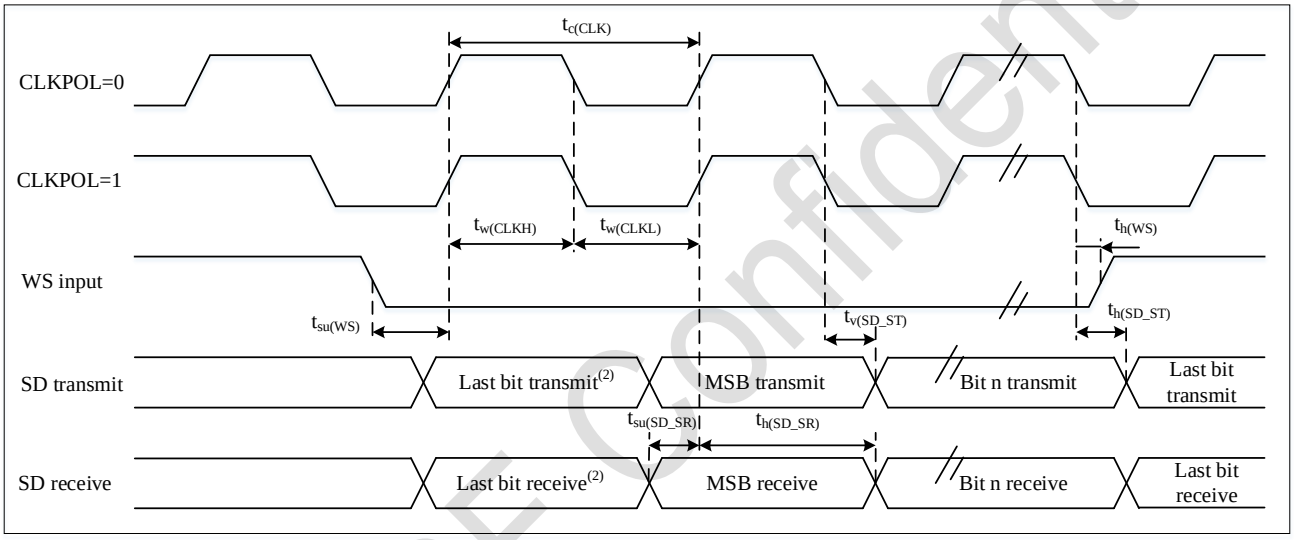


Figure 1-13. I²S Slave Mode Timing Diagram (Philips Protocol)(1)

1. The measuring points are set at the CMOS level: 0. 3 V_{DD} and 0. 7 V_{DD}.
2. Send/receive the lowest bit of the previous byte. There is no send/receive at the lowest level until the first byte.

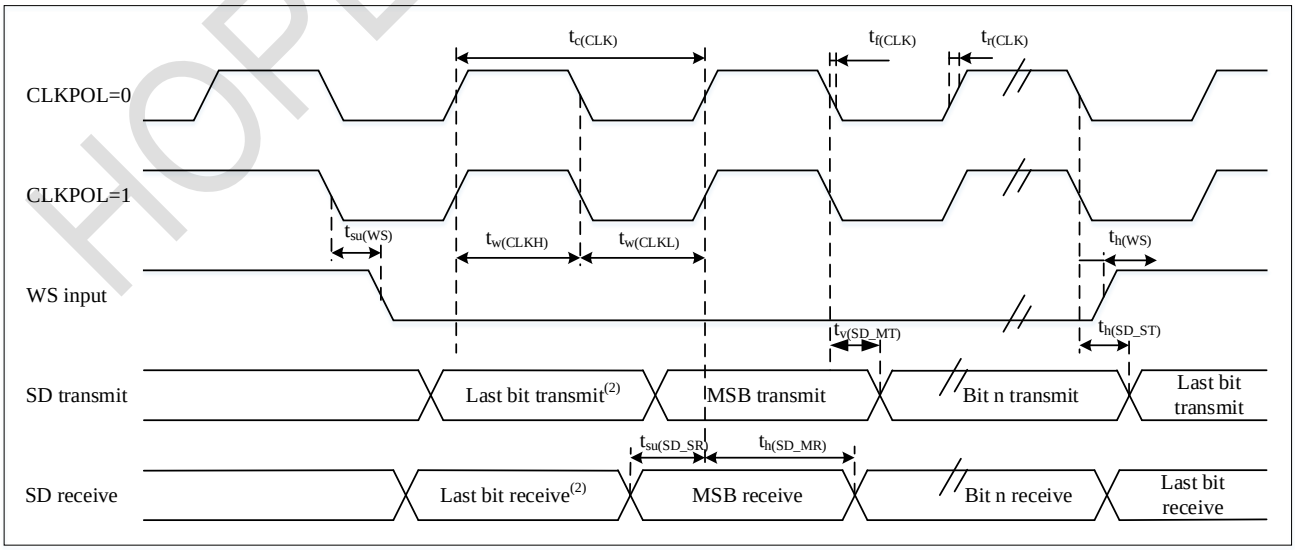


Figure 1-14. I²S Master Mode Timing Diagram (Philips Protocol)(1)

1. The measuring points are set at the CMOS level: 0.3 V_{DD} and 0.7 V_{DD} .
2. Send/receive the lowest bit of the previous byte. There is no send/receive at the lowest level until the first byte.

1.22 ADC Characteristic

Table 1-34. ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.4	3.3	5.5	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	-	-	18	MHz
f_s(1)	Sampling rate	-	-	0.89	1.33	Msps
V_{AIN}	Conversion voltage range (2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	See formula 1			Ω
R_{ADC}(1)	ADC input resistance	V_{DDA} =3.0 v	-	1500	-	Ω
C_{ADC}(1)	Internal sample and holding capacitor	-	-	13	15	pF
SNDR	Signal noise distortion ration	V_{DDA} =3.3 v	-	68	-	dB
t_S(1)	Sampling time	-	6	-	-	$1/f_{ADC}$
t_{STAB}(1)	Power-on time	-	32	-	-	$1/f_{ADC}$
t_{CONV}(1)	Conversion time	-	12			$1/f_{ADC}$

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. VREF+ is internally connected to VDDA。

Formula 1：maximum RAIN formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula is used to determine the maximum impedence so that the error can be less than 1/4 LSB, where N=12 (representing 12 bit resolution).

Table 1-35. ADC Accuracy(1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
EG	Gain error	V_{REF+} = 3.3 V， T_A = 25 °C， Vin = 0.05 V_{DDA}~ 0.95 V_{DDA}	±2	±5	LSB
EO	Offset error		±0.5	±2.0	
ED	Differential linearity error		±0.6	1.5	
EL	Integral linearity error		±1.5	2.5	
ENOB	Effective number of bits		11	-	Bits

1. DC numerical accuracy of the ADC is measured after internal calibration.

2. Relationship between the reverse injection current and ADC accuracy: it is needed to avoid reverse current injected on any standard analog input pin, as this will significantly reduce conversion accuracy of the other ongoing analog input pin . It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current.

3. Guaranteed by design and comprehensive evaluation, not tested in production.

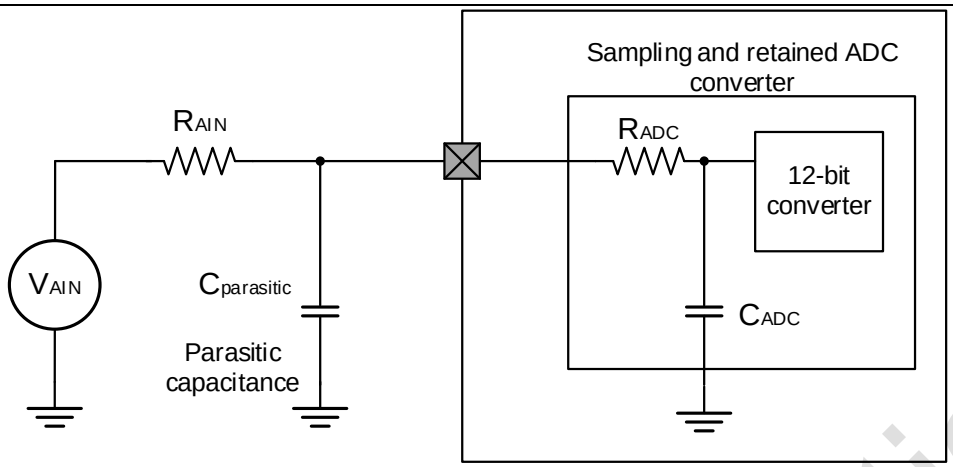


Figure 1-15. ADC Typical Connection Diagram

1.23 Operational Amplifier (OPAMP) Characteritic

Table 1-36. OPAMP Characteritic

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analog supply voltage	-	2.4	-	5.5	V
CMIR	Common mode voltage input range	-	0	-	VDDA	V
VIOFFSET	Input offset voltage	-	-	4	-	mV
ILOAD	Drive current	-	-	0.5	-	mA
IDDA	OPAMP current consumption Common mode rejection ratio	No load, quiescent mode	-	0.5	-	mA
CMMR	Power supply rejection ratio	-	-	70	-	dB
PSRR	Gain bandwidth	-	-	60	-	dB
GBW	Conversion rate	-	-	2.5	-	MHz
SR	Minimum impedance load	-		3	-	V/us
RLOAD	Maximum capacitive load	-	10	-	-	KΩ
CLOAD	Startup time	-	-	-	25	pF
TSTARTUP	Analog supply voltage	CLOAD ≤ 25 pf, RLOAD ≥ 10 kΩ, Follower configuration	-	3	5	μs
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 25 pF, Rload = 10 KΩ	-	1	-	MHz
		GA Gain = 4, Cload = 25 pF, Rload = 10 KΩ	-	0.5	-	
		GA Gain = 16, Cload = 25 pF, Rload = 10 KΩ	-	0.125	-	
		GA Gain = 32, Cload = 25 pF, Rload = 10 KΩ	-	0.0625	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.24 COMP Characteristic

Table 1-37. COMP Characteristic

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VDDA	Analog supply voltage	-		2.2	-	5.5	V
VIN	Input voltage range	-		0	-	VDDA	
TSTART	Comparator startup time	normal mode		-	-	5	us
		low speed mode		-	-	15	
td	Propagation delay for 200 mV step with 100 mV overdrive	VDDA>=2.2 V normal mode		-	100	-	ns
		low speed mode		-	520	-	
VOFFSET	Comparator input offset error	Full common mode range		-	±4	±20	mV
Vhys	Comparison of hysteresis voltage (high speed/low power consumption)	No hysteresis		-	0	-	mV
		Low hysteresis		-	10/8	-	
		Medium hysteresis		-	20/15	-	
		High hysteresis		-	30/25	-	
IDDA	Comparator current consumption	High speed mode	Static	-	35	-	µA
			With 50 kHz ±100 mV overdrive square signal	-	36	-	
		Low speed mode	Static	-	5	-	
			With 50 kHz ±100 mV overdrive square signal	-	6	-	

1. Guaranteed by design and comprehensive evaluation, not tested in production.

1.25 Temperature Sensor (TS) Characteristics

Table 1-38. Temperature Sensor Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±2	-	ºC
Avg Slope(1)	Average slope	-	3.9	-	mV/ºC
V_{25}(1)	Voltage at 25ºC	-	1.3	-	V
t_{START}(1)	Startup time	-	11	22	μs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature	-	1.87	6.43	μs

1. Guaranteed by design and comprehensive evaluation, not tested in production.
2. The shortest sampling time can be determined by the application through multiple cycles.

1.26 Rx Current vs. Data Rate

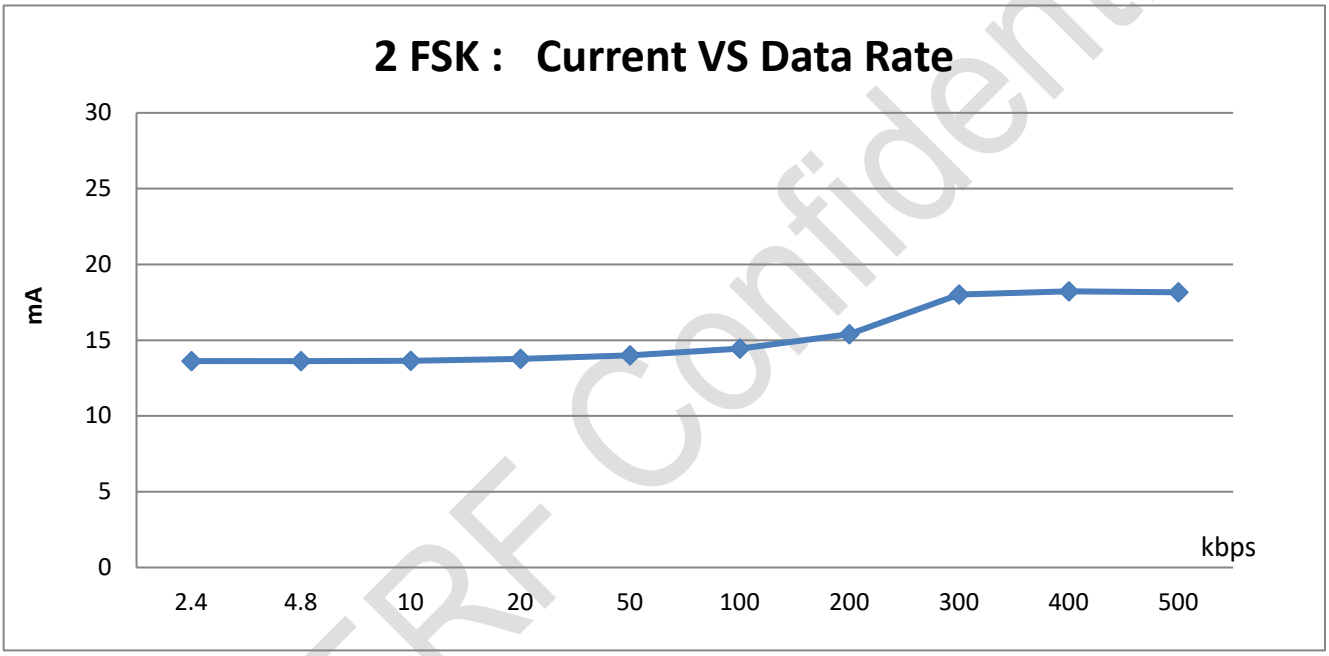


Figure 1-16. Rx Current vs Data Rate

Test Condition：Freq=434 MHz , ppm =10

1.27 Rx Sensitivity vs. Data Rate

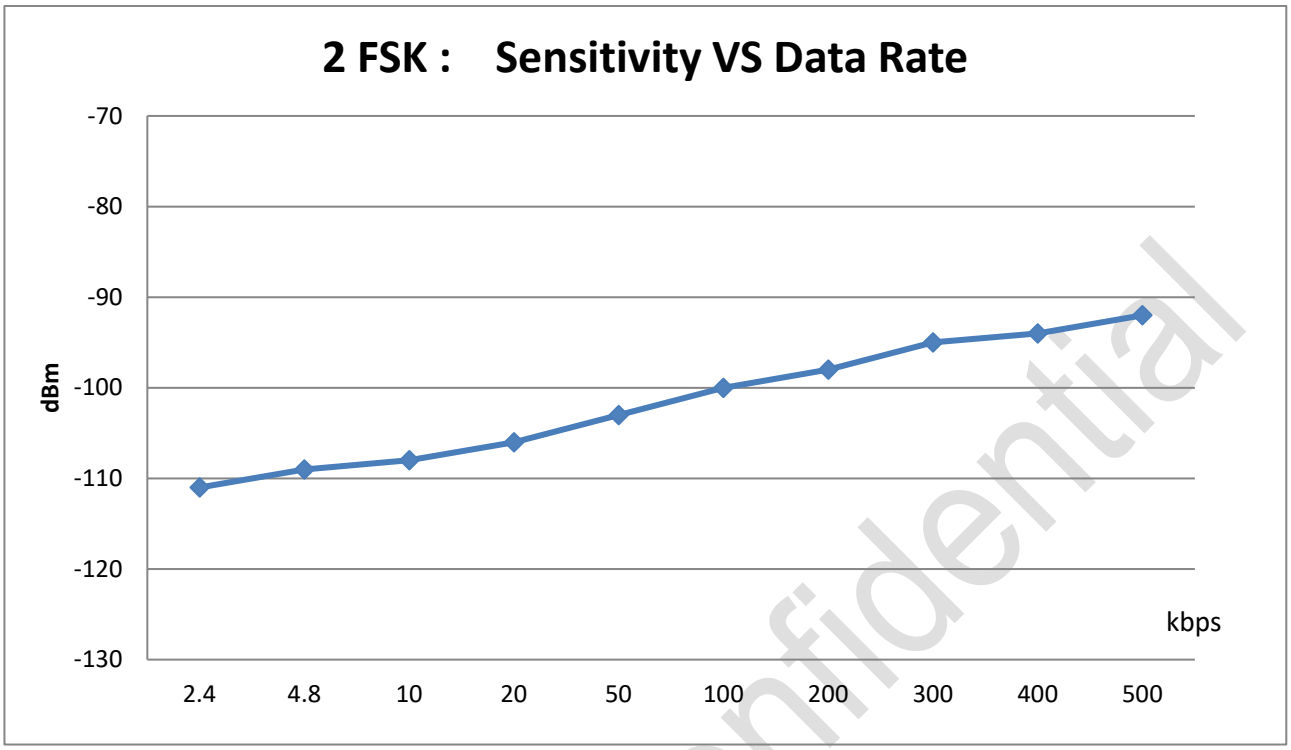


Figure 1-17. Rx Sensitivity vs Data Rate

Test condition: Freq = 434 MHz, ppm = 10, BER <=0.1%

1.28 Tx Power vs. Supply Voltage

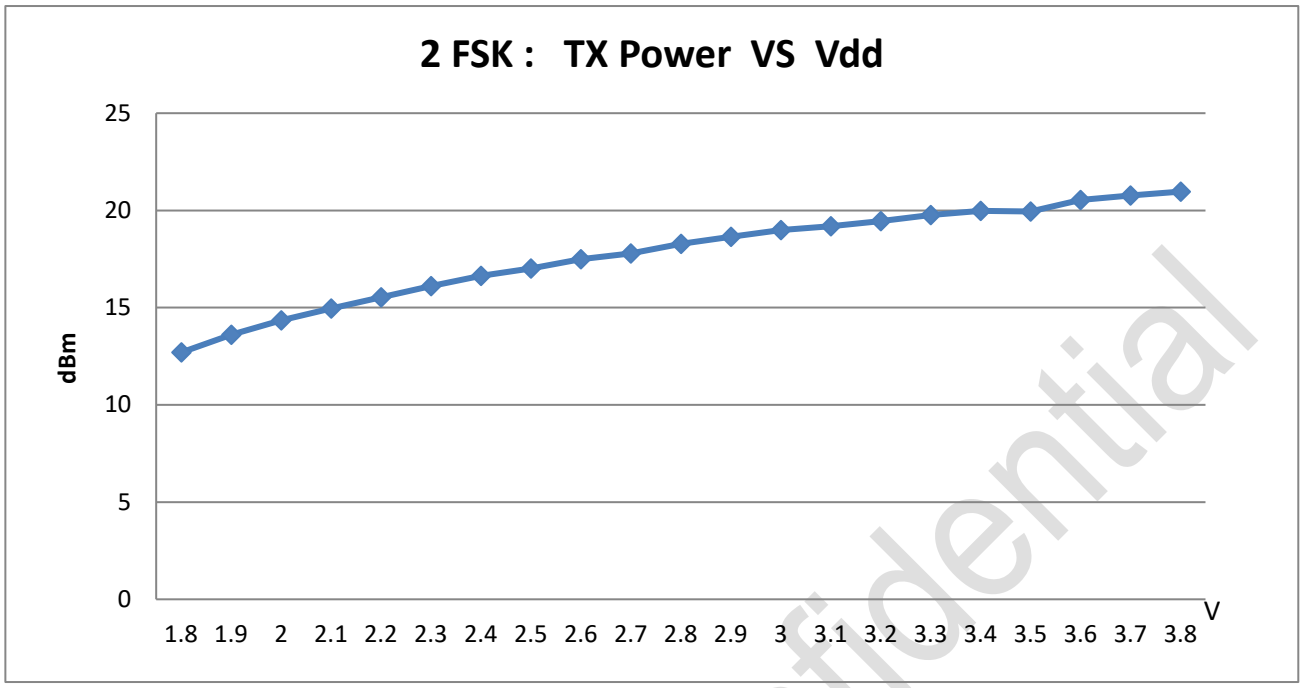


Figure 1-18. Tx Power vs Supply Voltage

Test condition: Freq = 434 MHz, 20 dBm matching network, Tx power with 3.3 V and 20 dBm

1.29 Tx Phase Noise

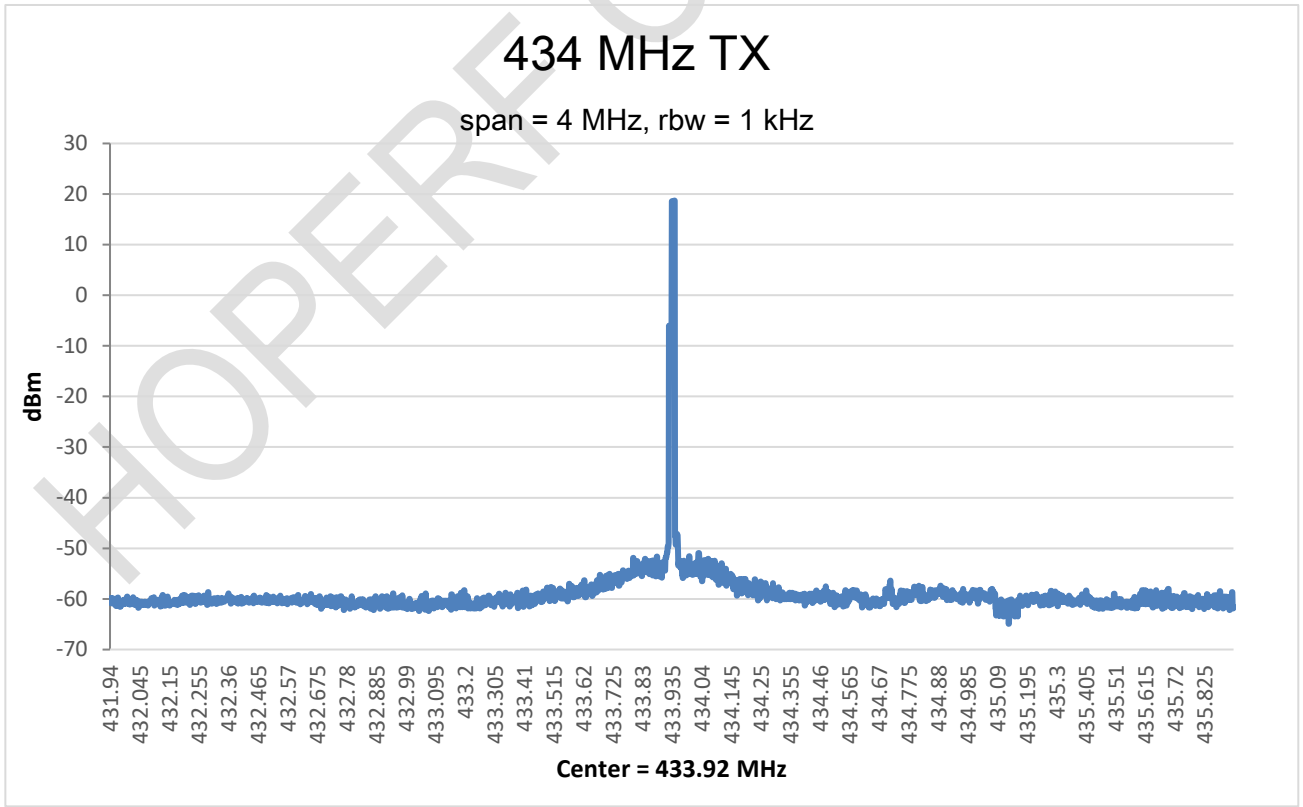


Figure 1-18. Tx Phase Noise

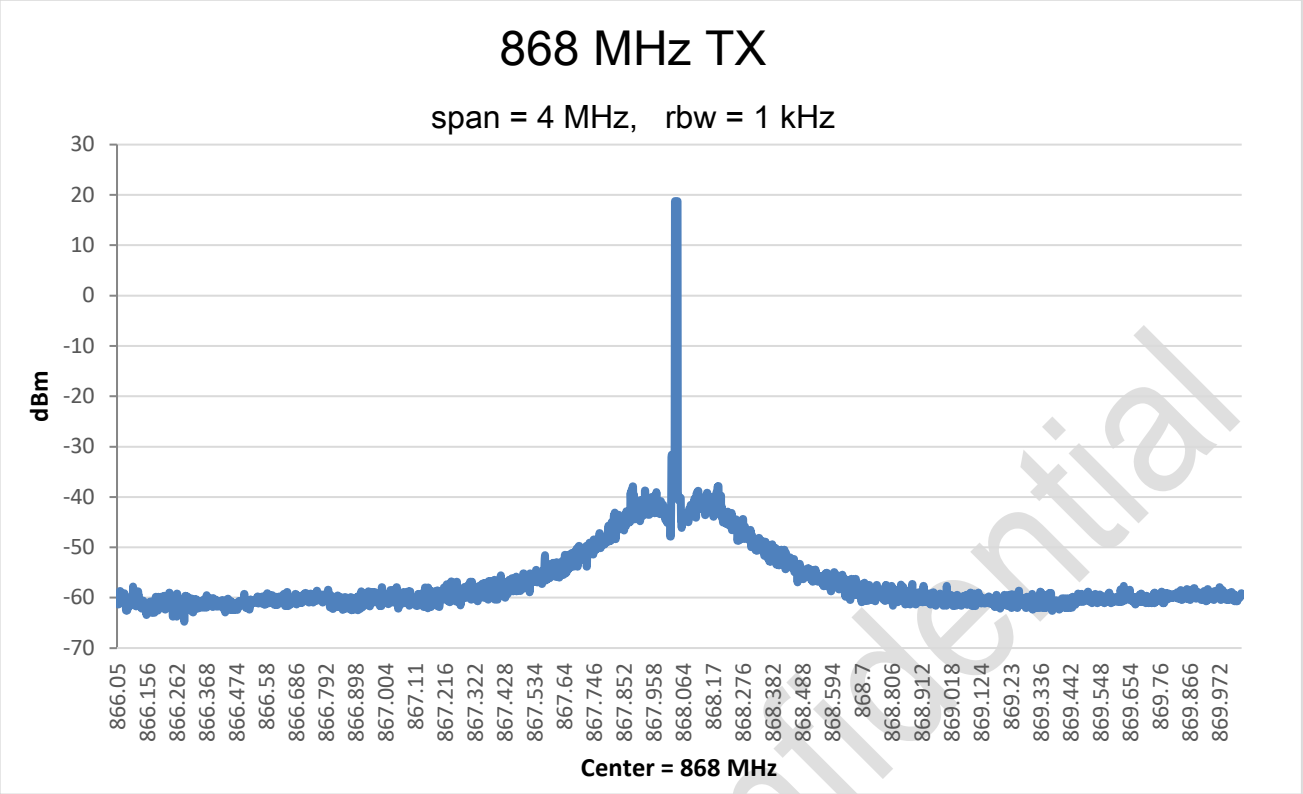


Figure 1-19. Tx Phase Noise

2 Pin Description

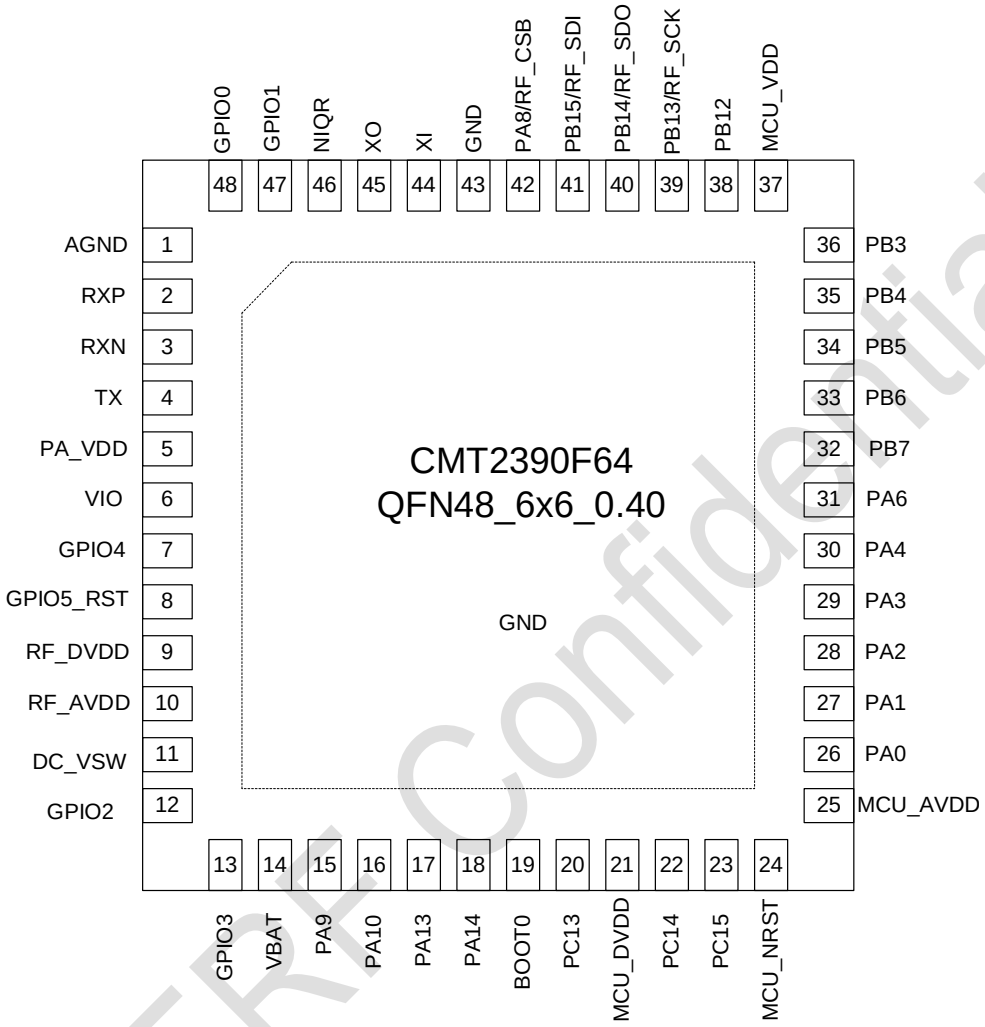


Figure 2-1. CMT2390F64 Pin Diagram

Table 2-1. CMT2390F64 Pin Description

Pin No.	Pin Name	I/O	Description
1	AGND	I	Anolog GND
2	RXP	I	RX signal input P
3	RXN	I	RX signal input N
4	TX	O	Output
5	PA_VDD	IO	PA VDD
6	VIO	IO	IO VDD
7	GPIO4	IO	Configurable
8	GPIO 5_RST	IO	Configurable
9	RF_DVDD	I	RF module digital VDD
10	RF_AVDD	I	RF circuit VDD
11	DC_VSW	I	DCDC

Pin No.	Pin Name	I/O	Description
12	GPIO2	IO	Configurable
13	GPIO3	IO	Configurable
14	VBAT	I	Anolog VDD
15	PA9	IO	MCU port PA9
16	PA10	IO	MCU port PA10
17	PA13	IO	MCU port PA13
18	PA14	IO	MCU port PA14
19	BOOT0		Boot memory selection
20	PC13	IO	MCU port PC13
21	MCU_DVDD	Analog	MCU positive digital power supply
22	PC14	IO	MCU port PC14
23	PC15	IO	MCU port PC15
24	MCU_NRST	I	MCU reset port, low level effective
25	MCU_AVDD	Analog	MCU positive analog power supply
26	PA0	IO	MCU port PA0
27	PA1	IO	MCU port PA1
28	PA2	IO	MCU port PA2
29	PA3	IO	MCU port PA3
30	PA4	IO	MCU port PA4
31	PA6	IO	MCU port PA6
32	PB7	IO	MCU port PB7
33	PB6	IO	MCU port PB6
34	PB5	IO	MCU port PB5
35	PB4	IO	MCU port PB4
36	PB3	IO	MCU port PB3
37	MCU_VDD	S	Supplymentary power supply
38	PB12	IO	MCU port PB12
39	PB13/RF_SCK	IO	MCU port PB13/ RF SPI clock
40	PB14/RF_SDO	IO	MCU port PB14 / RF SPI data output
41	PB15/RF_SDI	IO	MCU port PB15 / RF SPI data input
42	PA8/RF_CSB	IO	RF SPI chip selected of the access register
43	GND	I	Substrate GND
44	XI	I	Crystal circuit input
45	XO	O	Crystal circuit output
46	NIRQ	I	Configurable
47	GPIO1	IO	Configurable
48	GPIO0	IO	Configurable

3 Chip Frame

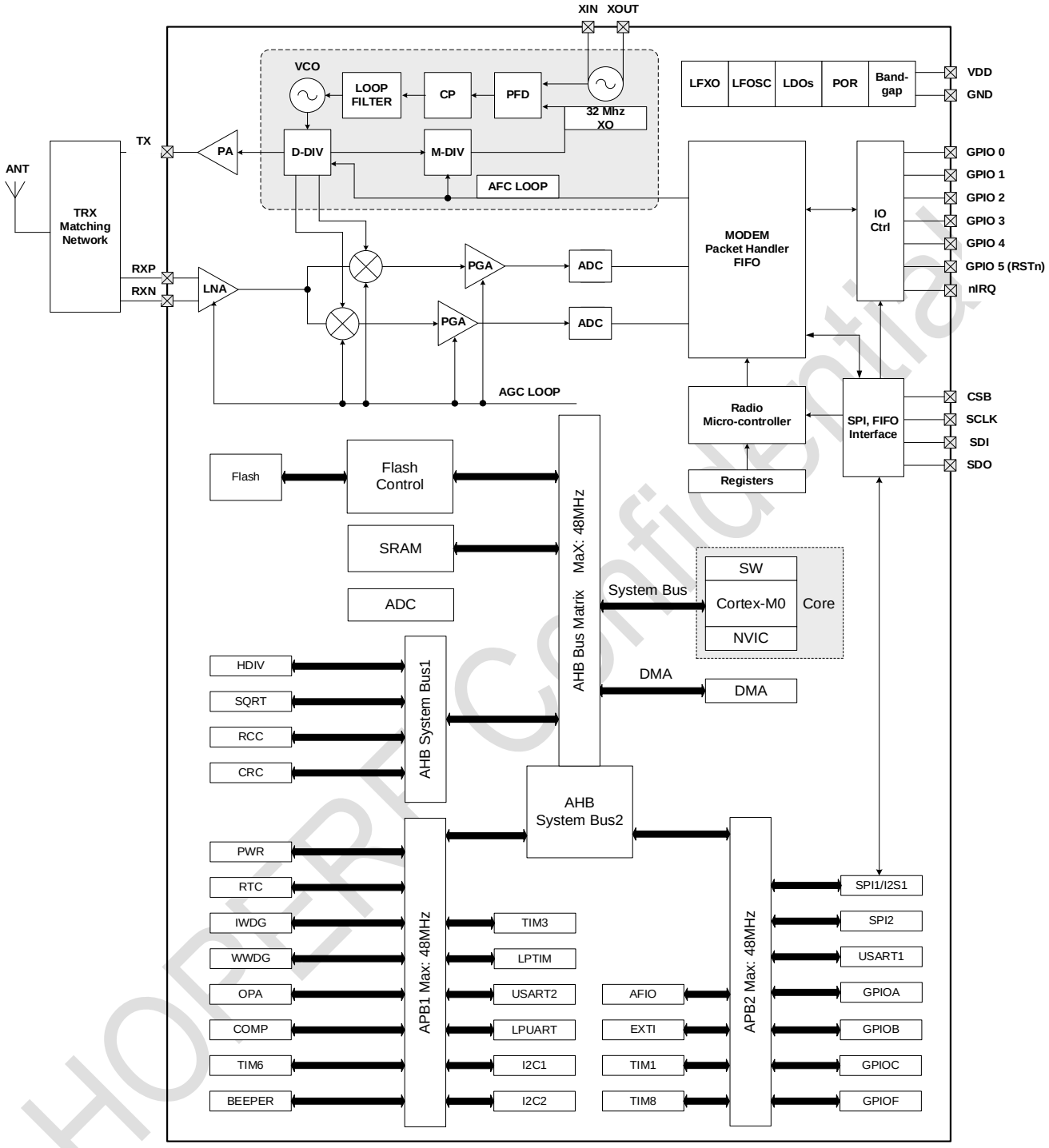


Figure 3-1. Functional Block Diagram

CMT2390F64 is an integrated Sub-G high-performance wireless transceiver single chip. The internal system block diagram of CMT2390F64 is shown in the above figure 3-1.

- **Low power high performance Sub-G transceiver**

Sub-G wireless transceiver supports 113 to 960 MHz, OOK, (G)FSK, 4 (G)FSK and other modulation modes, low power consumption, high performance, suitable for all kinds of wireless communication applications. The product belongs to CMOSTEK Next GenRF™ series, which includes transmitters, receivers and transceivers and other complete product series.

- **ARM Cortex-M0 high performance 32e bit micro-processor**

The CMT2390F64 controller uses a 32-bit ARM Cortex®-M0 kernel, with a maximum operating frequency of 48MHz, up to 64 KB encrypted Flash memory, and a maximum of 8 KB SRAM. It has a built-in high-speed AHB bus, two low-speed peripherals APB and bus matrix, supports up to 23 general I/O, provides a wealth of high-performance analog interface, including a 12-bit 1 Msps ADC. Besides, it supports up to 12 external input channels, 1 independent operational amplifier, 1 high-speed comparator, and provides a variety of digital communication interfaces, including three U(S)ART, two I2C, two SPI, and one I2S.

CMT2390F64 resources are shown as the following table.

Table 3-1. CMT 2390F64 External Resources

Project Name		CMT2390F64 External Resources	Notes
Flash capacitance (KB)		64	
SRAM capacitance (KB)		8	
CPU kernal and frequency		ARMCortex-M0 @ 48MHz	
Operating environment		1.8~3.6V / -40~+85℃	
Timer	General	3	
	High level	16 interrupt sources, 4 level priority	
	Basic	Enhance serial port	
	LPTIM	Support	
	RTC	Support	
Communication interface	SPI	Support	
	I2S	Support	
	I2C	Support	
	USART	Support	
	LPUART	Support	
GPIO		23	4 of them are connected to the RF of SPI
DMA		5-channel	
12 bit ADC		6-ch	1 Msps
OPA/COMP		1 / 1	
Beeper		1	TWI & STWI
Algorithmic support		CRC 16 / CRC 32	
Security protect		Read/write protect (RDP / WRP), Storage encryption	

4 Sub-G Transceiver

4.1 Transmitter

The CMT2390F64 transmitter is based on direct frequency synthesis technology. The carrier is generated by a low noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, step by step from -10 dBm to +20 dBm with 1 dB.

In OOK mode, when PA is switched on and off rapidly according to the transmitted data, it is easy to cause spectral spurts and burrs near the carrier. These spurts and burrs can be minimized by a Ramping mechanism. In FSK mode, CMT2390F64 supports signal transmission after Gaussian filtering, namely GFSK, so that the transmission spectrum is more concentrated. According to different application requirements, users can design a PA matching network to optimize the transmitting efficiency.

The transmitter can operate in direct mode and packet mode. In direct mode, the data can be sent to the chip by the DIN pin and transmitted directly. In the packet mode, the data can be pre-loaded into theTX FIFO in STBY state, and transmitted together with other package elements. Data can only be transmitted from FIFO in 4 FSK mode.

4.2 Receiver

CMT2390F64 has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broad band power detector and attenuation network nearby LNA, so as to obtain the best system linearity,selectivity, sensitivity and other performance.

Owing to CMOSTEK's low power design technic, the receiver consumes very low power when it is turned on.The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

Similar to the transmitter, the CMT2390F64 receiver can operate in direct mode and packet mode. In the direct mode,the demodulator output data can be directly output through the DOUT pin of the chip.DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and is filled in the FIFO. MCU can read the FIFO by the SPI interface.

4.3 Power-on Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2390F64 system. After the POR, the MCU must go through the initialization process and re-configure the CMT2380F64. There are two circumstances which will lead to the generation of POR.
The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9 V +/-20% (e.g.0.72 V–1.08 V) within 2 us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD as shown in the below figure.

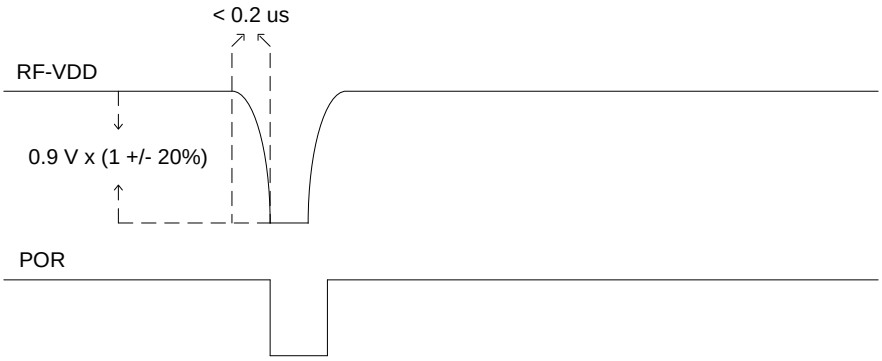


Figure 4-1. POR Reset Causing from Sudden Decreasing

The second case is,a slow decrease of the VDD. The POR triggering conditionis, RF-VDD decreases to 1.45 V+/-20% (e.g.1.16 V–1.74 V) within no less than 2 us. To be noticed, it detects absolute value of RF-VDD rather than decreasing amplitude. This situation is shown as below:

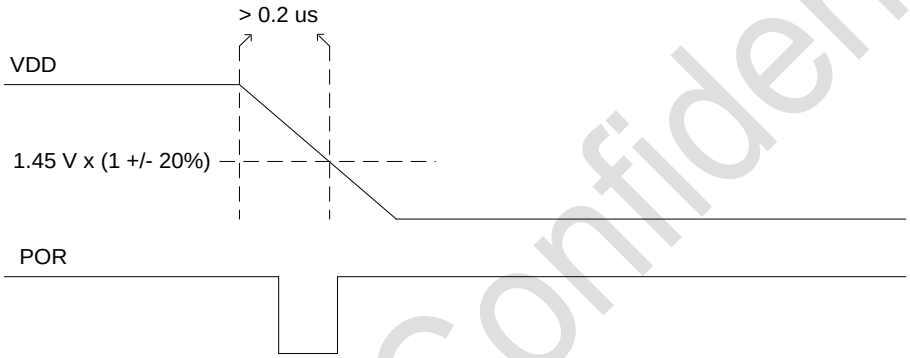


Figure 4-2. POR Reset Causing from Slow Decreasing

4.4 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL to make the crystal accurately oscillate at 32 MHz.

$$C_L = \frac{C_{on_{chip}} + C_{off\_chip} + C_{par}}{2}$$

The Conchip is the Load capacitor mounted to the ground at both ends of the crystal provided inside the CMT2390F64. The Conchip can be configured with the Xtal Cap Load on the RFPDK to be adjustable from 23 to 29 pF, and the step is about 190 fF. Coffchip is the load capacitor that connects both ends of the external crystal to the ground, which can be chosen by customers whether to increase it or not. Cpar is the parasitic capacitance from both ends of the crystal to the ground, which is about 2 ~ 6 pF. A 15 pF loaded crystal oscillator is recommended for use with the CMT2390F64. In addition, the lower the ppm of the crystal, the better the receiver performance.

4.5 Low Power Frequency Oscillator (LPOSC)

The CMT2390F64 RF system integrates a sleep timer driven by a 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer periodically wakes the chip from sleep. When the chip is operating in periodic operation mode, the sleep time can be configured from 62.5 us to 8585740.288 s. Since the frequency of the low power oscillator will drift with temperature and voltage, it will be automatically calibrated during the power-up phase and will be periodically calibrated. These calibration will keep the frequency tolerance of the oscillator within 1%.

4.6 Internal Low Power Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, the test is performed once. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_DATA register.

4.7 Received Signal Strength Indicator (RSSI)

RSSI is used to evaluate the signal strength inside the channel with detection range from –127dBm to 20 dBm. Users can Users can configure the RSSI Detect Mode in RFPDK to choose whether to output the RSSI value in real time or to lock the RSSI value at each stage when receive data packets.

CMT2390F64 allows users to setup a threshold RSSI Compare TH in RFPDK to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic 1, otherwise, it outputs logic 0. The results can be output to RSSI VLD interrupt and to assist the operation of internal super-low power (SLP) mode.

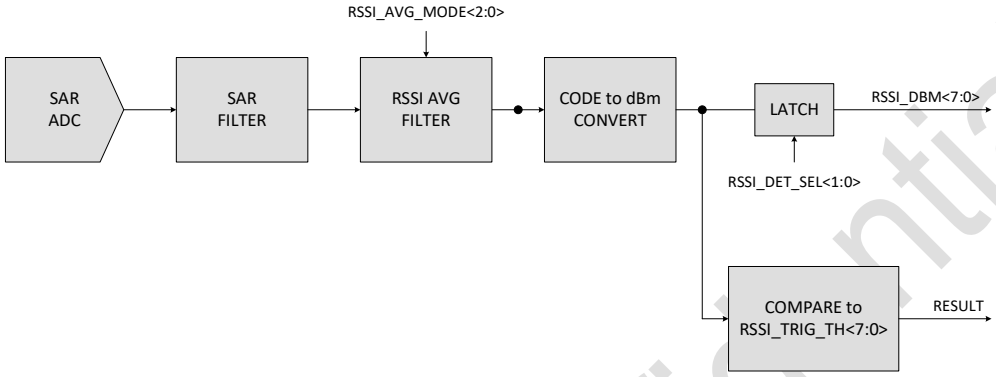


Figure 4-3. RSSI Measurement and Comparison Circuit

CMT2390F64 has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, users need to recalibrate the RSSI circuit in their dedicated applications. For further information, please refer to the *AN144-CMT2300A RSSI Usage Guide.*

4.8 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in 2-FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to identify whether it is a wanted signal or an unwanted noise. OOK and 4-FSK demodulation do not support this function

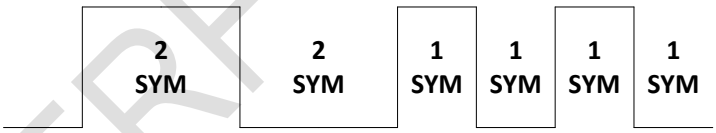


Figure 4-4. Received Signal Jump Diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal. As shown in the above figure, although 8 symbols are received, only 6 phase jumps appeared 6. Therefore, the number of jumps is not equal to the number of symbols. Only when preamble is received, the jumps and signal numbers are equal. In general, the more jumps are used to identify the signal, the more reliable the result is; the less jumps are used, the faster the result is obtained. If the RX timeis set to are latively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g. the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa.

Detecting the phase jump of a signal, is identical to detect whether the signal is the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is valid, as well as to see if the SNR is over 7 dB. According to detect result of the data rate and the Deviation as well as SNR, if it is detected as a reliable signal, it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in thesuper low power (SLP) mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, while more reliable. When users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.9 Clock Data Recovery（CDR）

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data. So

CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.
CMT2390F64 has designed three types of CDR systems, which is shown as followed:

- **COUNTING system** – The system is designed for the symbol rates to be more accurate. If the symbol rate is100% aligned, the unlimited length of 0 can be received continuously without error.
- **TRACING system** – The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted byTX, and adjust quickly the local symbol rate of RX at the sametime, so as to minimize the error between them. The system can withstand up to 15.6% symbol rate error. Other similar products in the industry cannot reach this level.
- **MANCHESTER system**–This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes

4.10 Fast Frequncy Hopping

The mechanism of fast frequency hopping is based on the frequency configured on the RFPDK, for instance, the MCU can simply set 1 or 2 registers to quickly switch to another frequency points during applications at 433.92 MHz. This simplifies the way of change the RX or TX frequency in multiple channels application.

$$\mathbf{FREQ = Base\ Freq + 1\ kHz \times FH\_OFFSET<7:0> \times FH\_CHANNEL<7:0>}$$

In general, users can configure FH_OFFSET<7:0> during the chip initialization process. And then in the application, users can switch the channel by changing FH_CHANNEL<7:0>.

4.11 Chip Operation

4.11.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface (FCSB、CSB、SDA、SCLK). It is defaulted set as 4-wire SPI and then configured as 3-wire after power on. The CSB is the active-low chip select signal for accessing to the registers. The SCLK is the serial clock. Its highest speed is 10 MHz.The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge. The SDI is for data input and SDO is for data output. In 3-wire mode, SDI is used for both data input and output, and SDO is idle. Both the address and data parts are transmitted from the MSB.
When accessing to the register, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCLK cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.
Noted that for the 4-wire register write operation below, while SDI writes data, SDO will output the current value of the register (old register read data), and the MCU can decide whether to read it as needed.

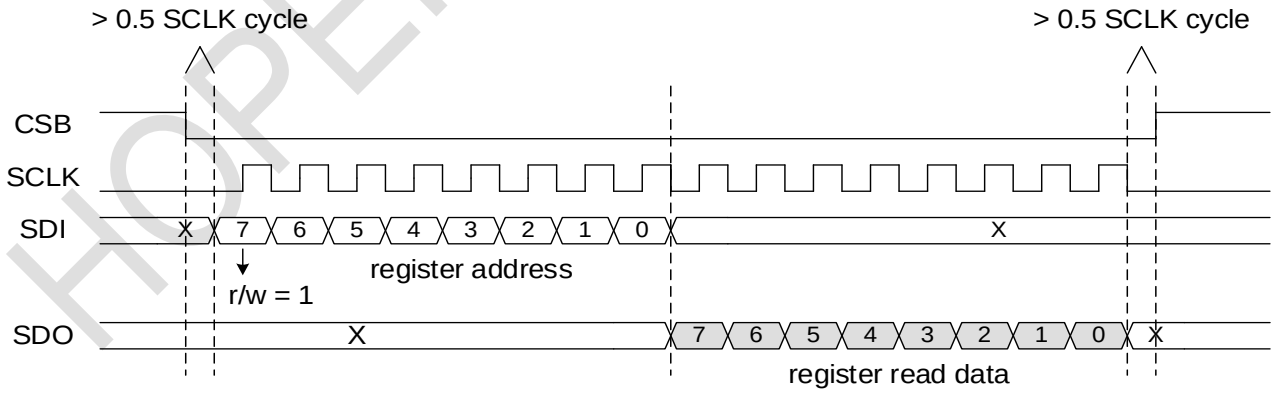


Figure 4-5. SPI Read Register Timing

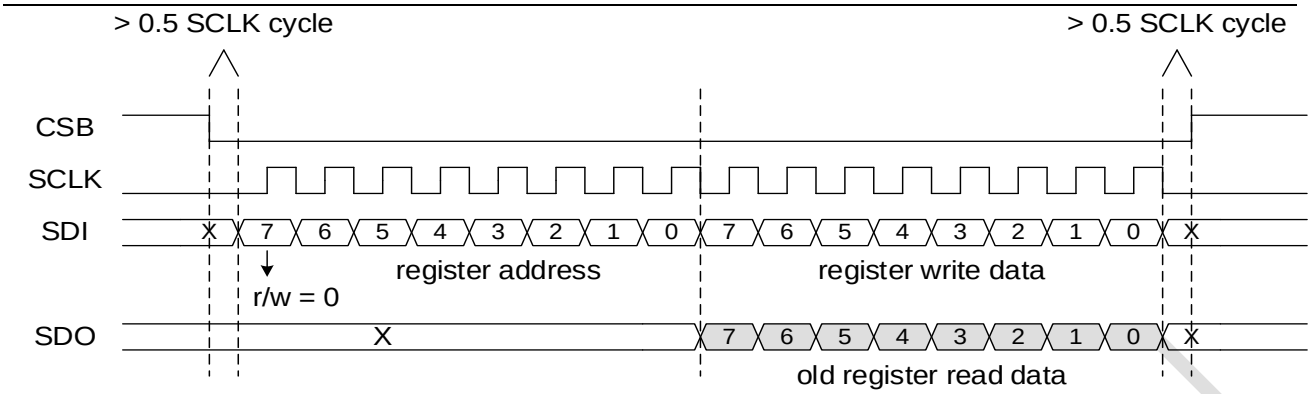


Figure 4-6. SPI Write Register Timing

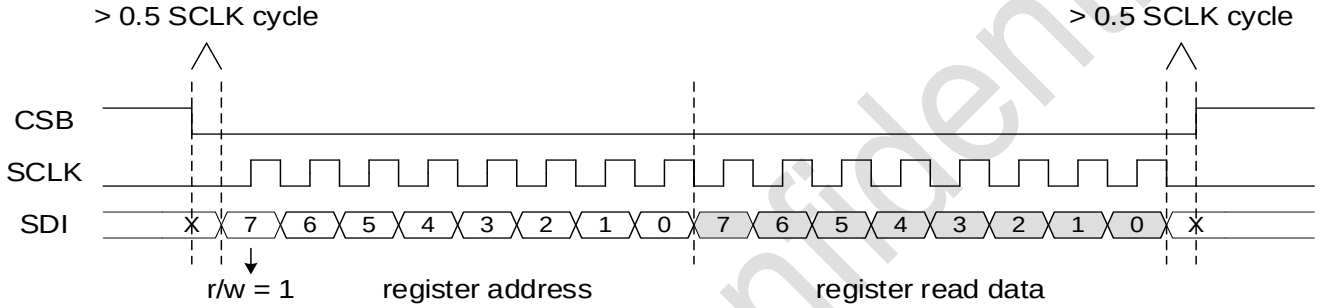


Figure 4-7. SPI (3-wire) Read Register Timing

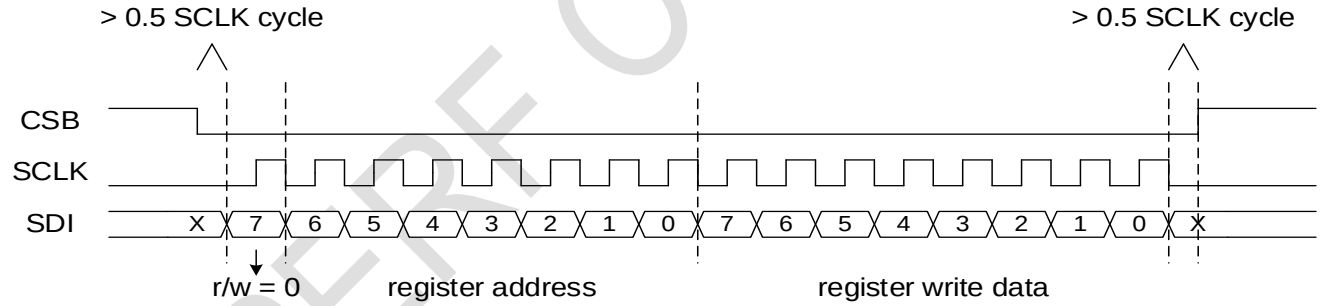


Figure 4-8. SPI (3-wire) Write Register Timing

For 3-wire read register, both MCU and CMT2390F64 will switch the IO (SDIO) port between address 0 and 7. At this point, CMT2390F64 will switch the IO port from input to output, and MCU will switch the IO port from output to input. Please note the dotted line in the middle. It is strongly recommended that MCU switch the IO port to input before sending out the falling edge of SCLK. The CMT2390F64 does not switch IO to output until a falling edge happened. This avoids the situation when both of the MCU and CMT2390F64 sets SDIO to output at the same time, which will result in electrical conflict. For some MCUs, this may cause a reset or other abnormal behavior.

4.11.2 FIFO Interface

CMT2390F64 provides two separated 128-byte FIFO by defaul for RX and TX respectively. RX FIFO is used to store the received data in RX mode and TX FIFO is used to store the transmitting data in TX mode. Users can also set FIFO_MARGE_EN to1 to merge the two separated FIFO into one 256-byte FIFO. It can be used both underTX and RX. By configuring the FIFO_RX_TX_SEL to indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the next time 128 byte TX FIFO while the 128 byte RX FIFO is filled in the RX mode to save operation time.

FIFO can be accessed via the SPI interface. Users can clear FIFO by setting FIFO_CLR_TX or FIFO_CLR_RX. Also, users can re-send the old data in FIFO_RESTORE without re-filling the data.

Users can configure PD_FIFO to control whether the FIFO saves content in the SLEEP mode. PD_FIFO = 0 means that FIFO can save contents in SLEEP state, but it will consume about 200 nA of leakage current.

When MCU accesses FIFO, users must first configure a few registers to set up the FIFO read/write mode, as well as some other working mode. Below is the read-write timing diagram. The FIFO operation is triggered by writing address 0x7A of Page 0. When r/w bit is 0, the FIFO operation is written, and when R/W bit is 1, the FIFO operation is read.

FIFO read and write can also be operated by using 3-wire SPI. When in 3-wire, read data output and write data input are carried out on the SDI pin. When in 4-wire, write data is input from SDI and read data is output from SDO. The FIFO operation process is to access the FIFO operation port at address 0x7A, where the read and write bits determine whether to write or read data at the following. For the following continuous read or write phase, it is up to users.

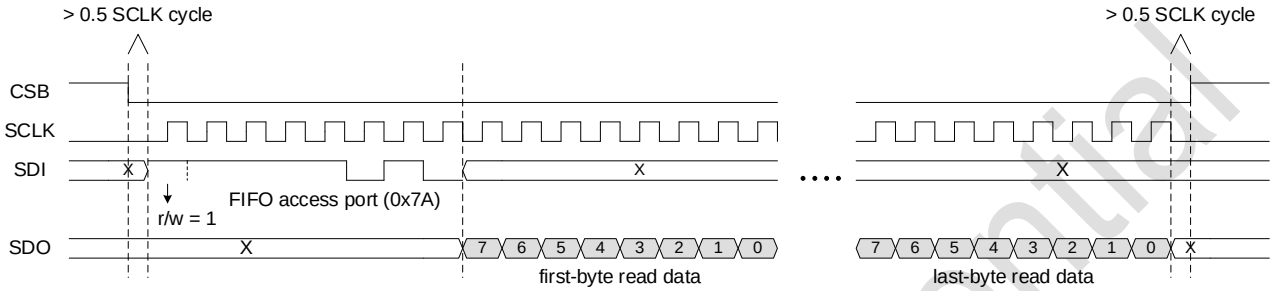


Figure 4-9. SPI (4-wire) Read FIFO Timing

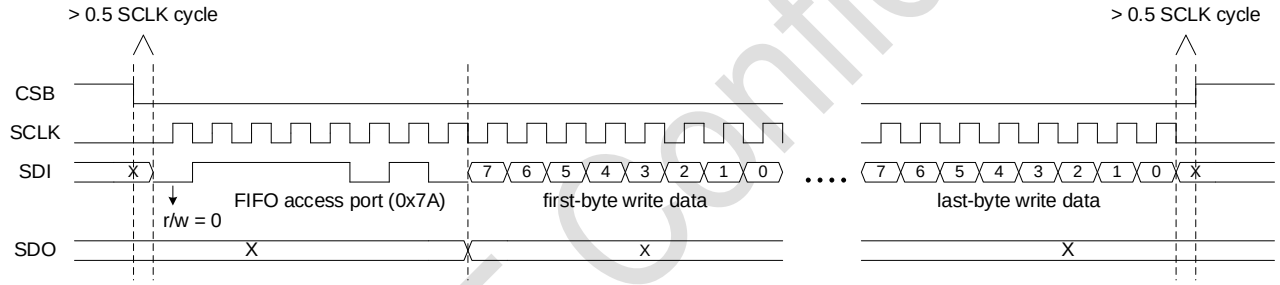


Figure 4-10. SPI (4-wire) Write FIFO Timing

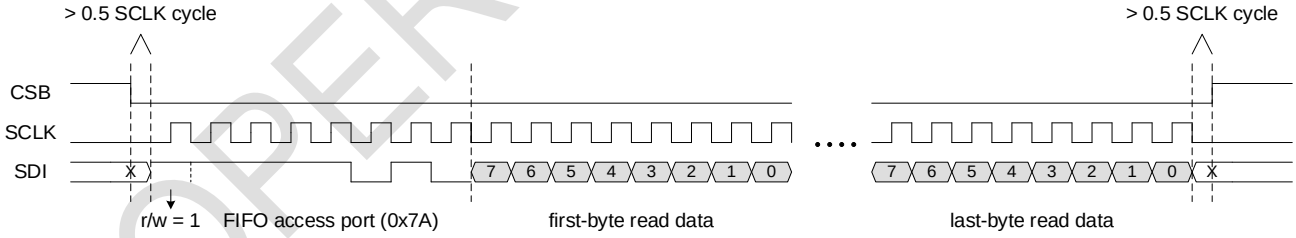


Figure 4-11. SPI (3-wire) Read FIFO Timing

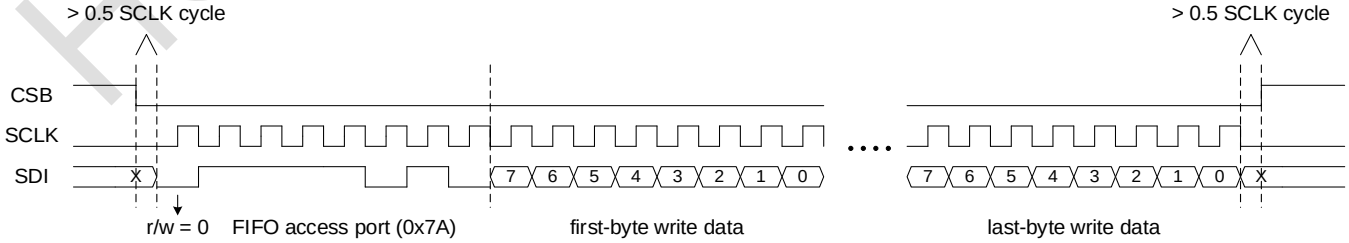


Figure 4-12. SPI (3-wire) Write FIFO Timing

Transceivers provide a numbers of FIFO related interrupt sources as auxiliary tools for efficient chip operation. The FIFO interrupt timing sequence related to Rx and Tx is shown in the figure below.

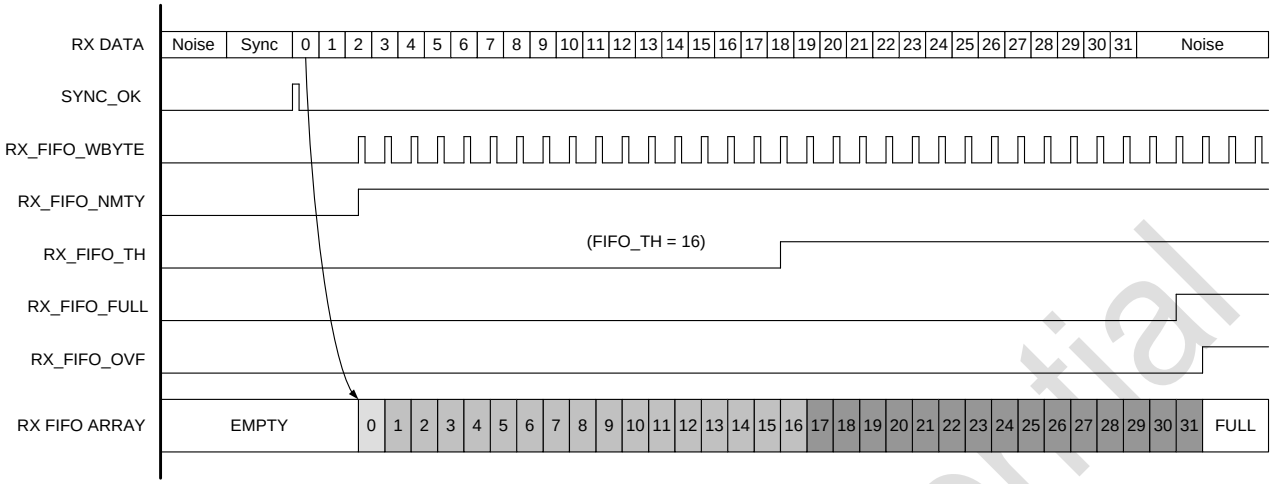


Figure 4-13. Transceiver RX FIFO Interrupt Sequence Diagram

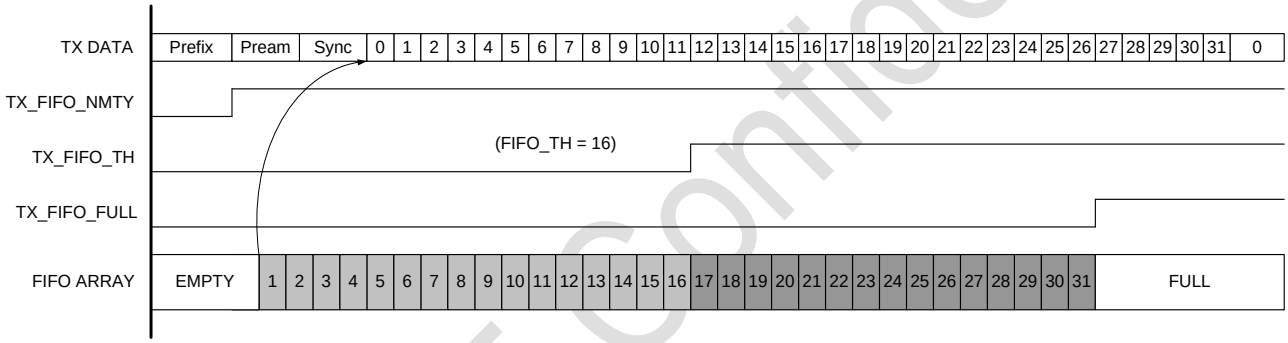


Figure 4-14. Transceiver TX FIFO Interrupt Sequence Diagram

4.11.3 Transceiver Working Status, Timing and Power Consumption

- Startup time

After the transceiver is powered on RF-VDD, it usually needs to wait for about 1ms until POR released. After the RELEASE of POR, the crystal will also start. The startup time is assumed to be N ms, which depends on the characteristics of the crystal itself. After startup, it is necessary to wait for the crystal to stabilize the system before starting to work. The default stability time is 2.48 ms, which can be written to XTAL_STB_TIME <2:0>; After modification, the chip will stay in IDLE state until the crystal is stable. After the crystal is stable, the chip will leave IDLE and start to do the calibration of each module. After the calibration, the chip will stay in SLEEP, waiting for the user to initialize the chip. The chip returns to IDLE and starts the power-on process again.

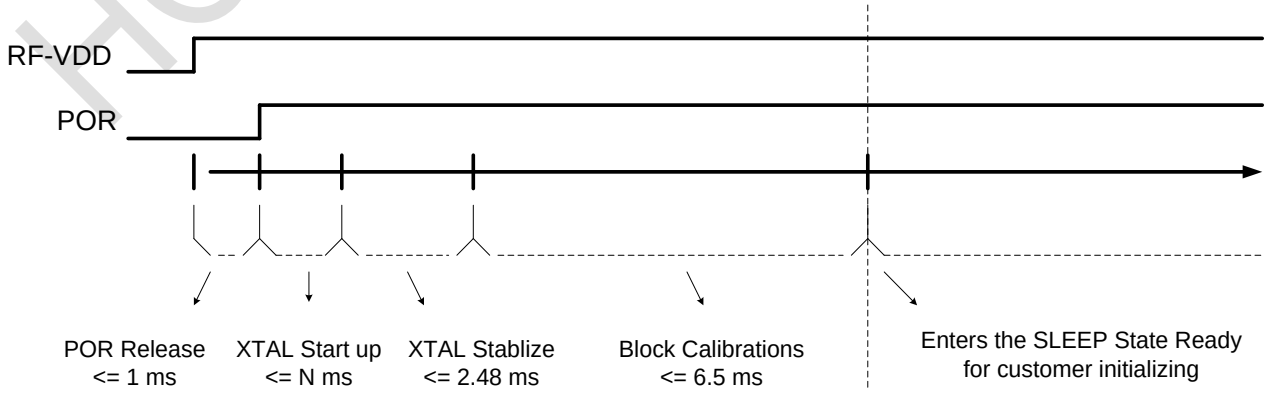


Figure 4-15. Power On Timing

The chip enters SLEEP state after calibration. And then, the MCU can control the chip to switch to different operation states through setting the register CHIP_MODE_SWT<7:0>.

- Operation State

CMT2390F64 has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below.

Table 4-1. Transceiver State and Corresponding Active Module

State	Binary code	Switch command	Active module	Optional module
IDLE	0x00	soft_rst	SPI, POR	None
SLEEP	0x81	go_sleep	SPI, POR	LFOSC, FIFO, Sleep Timer
READY	0x82	go_ready	SPI, POR, XTAL, FIFO	None
RFS	0x84	go_rfs	SPI, POR, XTAL, PLL, FIFO	None
TFS	0x88	go_tfs	SPI, POR, XTAL, PLL, FIFO	None
RX	0x90	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+ADC, FIFO	RX Timer
TX	0xA0	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	None

The following table lists the time it takes to switch states, with the starting states listed on the left:

Table 4-2. Transceiver State and State Switching Time

	Ideal State					
Starting State	**SLEEP**	**READY**	**RFS**	**RX**	**TFS**	**TX**
SLEEP		660 us	770 us	820 us	770 us	820 us
READY	Immediately		110 us	160 us	110 us	160 us
RFS	Immediately	Immediately		20 us	Cannot switch	Cannot switch
RX	Immediately	Immediately	Immediately		Cannot switch	160 us
TFS	Immediately	Immediately	Cannot switch	Cannot switch		20 us
TX	Immediately	Immediately	Cannot switch	160 us	Immediately	

Note：

In Direct mode, if the chip is in transmission, it will exit TX state as it receives command of switching.
In Packet mode, if the chip is in transmission, it will exit TX state after transmission complete must complete.

Below shows the state switching diagram and status signal：

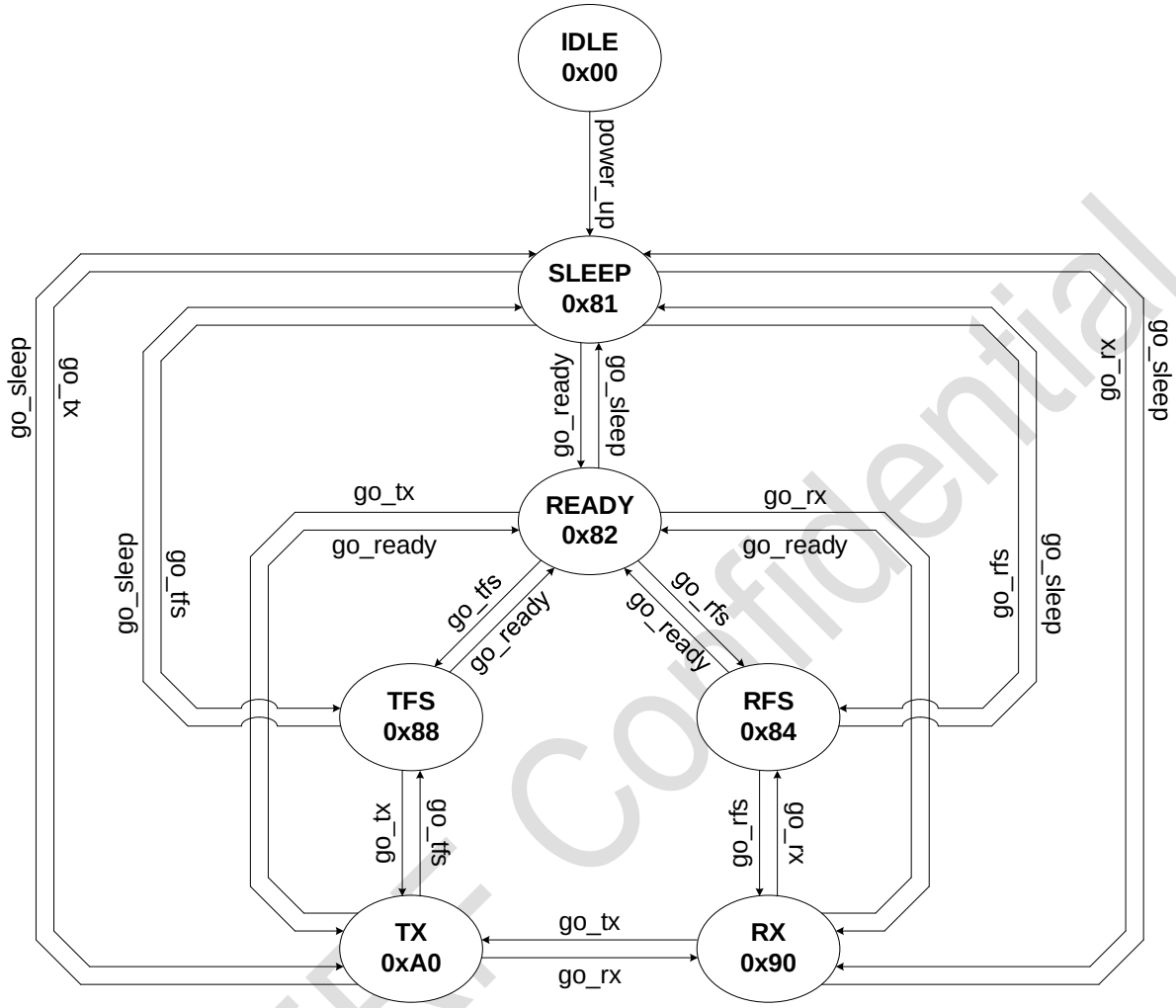


Figure 4-12. State Switch Diagram

➢ SLEEP State

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged. However, users cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

➢ RFS State

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching from STBY to RFS probably requires PLL calibration and stability time of 350 us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

➢ TFS State

TFS is a transition state before switching to TX. Except that the transmitter RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from STBY to TFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to TFS needs to add the crystal start-up and settled time. Switching from other state to TFS will be completed immediately.

➢ RX State

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20 us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully.

➢ TX State

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20 us. Switching from STBY to TX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350 us to switch successfully. GPIO Function and Interrupt Mapping

CMT2390F64 has 7 GPIO ports（GPIO0～GPIO5 and NIRQ）. Each GPIO can be configured as a different input or output. CMT2390F64 has 3 interrupt ports（INT1、INT2、INT3）. They can be configured to different GPIO mapping output.

Table 4-3. CMT2390F64 GPIO Function

Pin No.	Pin Name	I/O	Function
48	GPIO0	IO	Can be configured as：DOUT，INT1，INT2，INT3，DCLK，TRX_SWT
47	GPIO1	IO	Can be configured as：DCLK，INT1，INT2，DOUT，TRX_SWT
12	GPIO2	IO	Can be configured as：INT1，INT2，INT3，DCLK，DOUT，ANTD1
13	GPIO3	IO	Can be configured as：INT1，INT2，DCLK，DOUT，DIN，ANTD2
7	GPIO4	IO	Can be configured as：DOUT，INT1，INT2，DCLK，DIN，CLKO，LFCLKO
8	GPIO5	IO	Can be configured as：RSTn，INT1，INT2，DOUT，DCLK
46	NIRQ	IO	Can be configured as：INT1，INT2，DCLK，DOUT，DIN，TCXO

Below shows the Interrupt mapping in table 4-4. INT 1 and INT 2 mapping is the same. Take INT 1 as an example.

Table 4-4. CMT 2390F64 Interrupt Mapping

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
INT_MIX	000000	Compounded interrupt, INT_MIX will be valid if any one of the interrupts below is enabled.	Auto/By MCU
ANT_LOCK	000001	Antenna lock interrupt is active after enabling the antenna diversity function.	By MCU
RSSI_PJD_VALID	000010	Interrupt valid for RSSI and/or PJD.	Auto
PREAM_PASS	000011	Successfully receive the Preamble interrupt.	By MCU
SYNC_PASS	000100	Successfully receive the Sync Word interrupt.	By MCU
ADDR_PASS	000101	Successfully receive the Addr interrupt.	By MCU
CRC_PASS	000110	Successfully receive interrupt of passing the CRC check.	By MCU
PKT_OK	000111	Successfully receive interrupt of receiving an entire and correct packet.	By MCU
PKT_DONE	001000	Indicates that the current data packet has been received with the following 4 cases. 1. A complete and correct packet is received. 2. Manchester decoding error occurs and the decoding circuit restarts automatically. 3. NODE ID receiving error occurs and the decoding circuit restarts automatically. 4. A signal conflict is found and the decoding circuit does not restart automatically but waits for the MCU to process.	By MCU
SLEEP_TMO	001001	Interrupt indicating SLEEP timer timeout.	By MCU
RX_TMO	001010	Interrupt indicating RX timer timeout.	By MCU

Name	INT1_SEL	Interrupt Descriptions	Clearing Method
RX_FIFO_NMTY	001011	Interrupt indicating RX FIFO is not full.	Auto
RX_FIFO_TH	001100	Interrupt indicating the unread content of RX FIFO exceeding FIFO TH.	Auto
RX_FIFO_FULL	001101	Interrupt indicating RX FIFO is full	Auto
RX_FIFO_WBYTE	001110	Interrupt generated every time a BYTE is written into RX FIFO, i.e., it is a pulse.	Auto
RX_FIFO_OVF	001111	Interrupt indicating RX FIFO is overflow	Auto
TX_DONE	010000	Interrupt indicating TX complete.	By MCU
TX_FIFO_NMTY	010001	Interrupt indicating TX FIFO is not full.	Auto
TX_FIFO_TH	010010	Interrupt indicating the unread content of TX FIFO exceeding FIFO TH.	Auto
TX_FIFO_FULL	010011	Interrupt indicating TX FIFO is full.	Auto
STATE_IS_READY	010100	Interrupt indicating that the current state is READY.	Auto
STATE_IS_FS	010101	Interrupt indicating that the current state is RFS or TFS.	Auto
STATE_IS_RX	010110	Interrupt indicating that the current state is RX.	Auto
STATE_IS_TX	010111	Interrupt indicating that the current state is TX.	Auto
LBD_STATUS	011000	Interrupt indicating that low voltage detection being active (VDD is lower than the set TH).	By MCU
API_CMD_FAILED	011001	Interrupt indicating API command execution error.	By MCU
API_DONE	011010	Interrupt indicating API command completion.	By MCU
TX_DC_DONE	011011	Interrupt for Duty Cycle TX mode complete	By MCU
ACK_RECV_FAILED	011100	Interrupt indicating ACK receiving failure.	By MCU
TX_RESEND_DONE	011111	Interrupt for repeated TX complete	By MCU
NACK_RECV	011110	Interrupt indicating receipt of NACK.	By MCU
SEQ_MATCH	011111	Interrupt indicating successful serial number matching.	By MCU
CSMA_DONE	100000	Interrupt for CSMA complete	By MCU
CCA_STATUS	100001	Signal channel sensing interrupt.	By MCU

Interrupt is enabled when register value is 1 by default. Users can set the INT_POLAR register bit to 1 to make all interrupts enabled when the register value is 0. Take INT1 as an example, the control and selection of two different types of interrupt sources is shown in the figure below. The control and mapping ofINT1 and INT2 is the same and both can be mapped to any GPIO.INT_MIX is the only source for INT3, which can only be mapped to GPIO0 and GPIO2. In application, users can choose either to map all interrupt sources to the interrupt port through INT_MIX (identify which interrupt is valid by checking the interrupt flag) or directly map a specific interrupt source to the interrupt port.

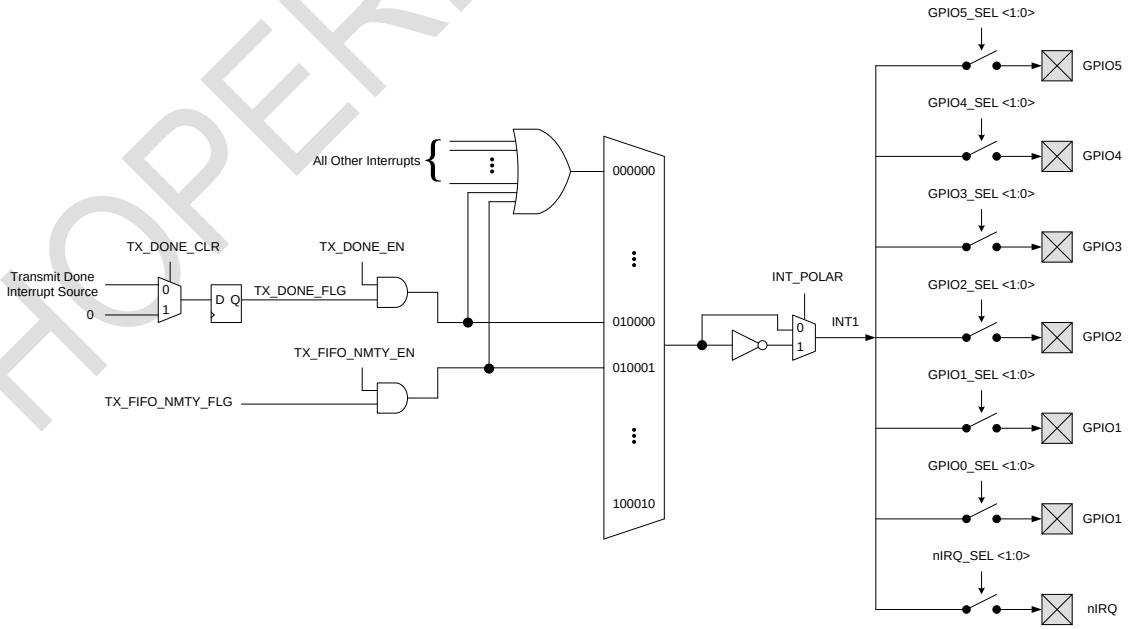


Figure 4-17. CMT2390F64 INT 1 Interrupt Mapping

5 Function Description

5.1 Memory

CMT2390F64 includes embedded encrypted flash memory (Flash) and embedded SRAM, Figure 5-1 below shows the memory address map.

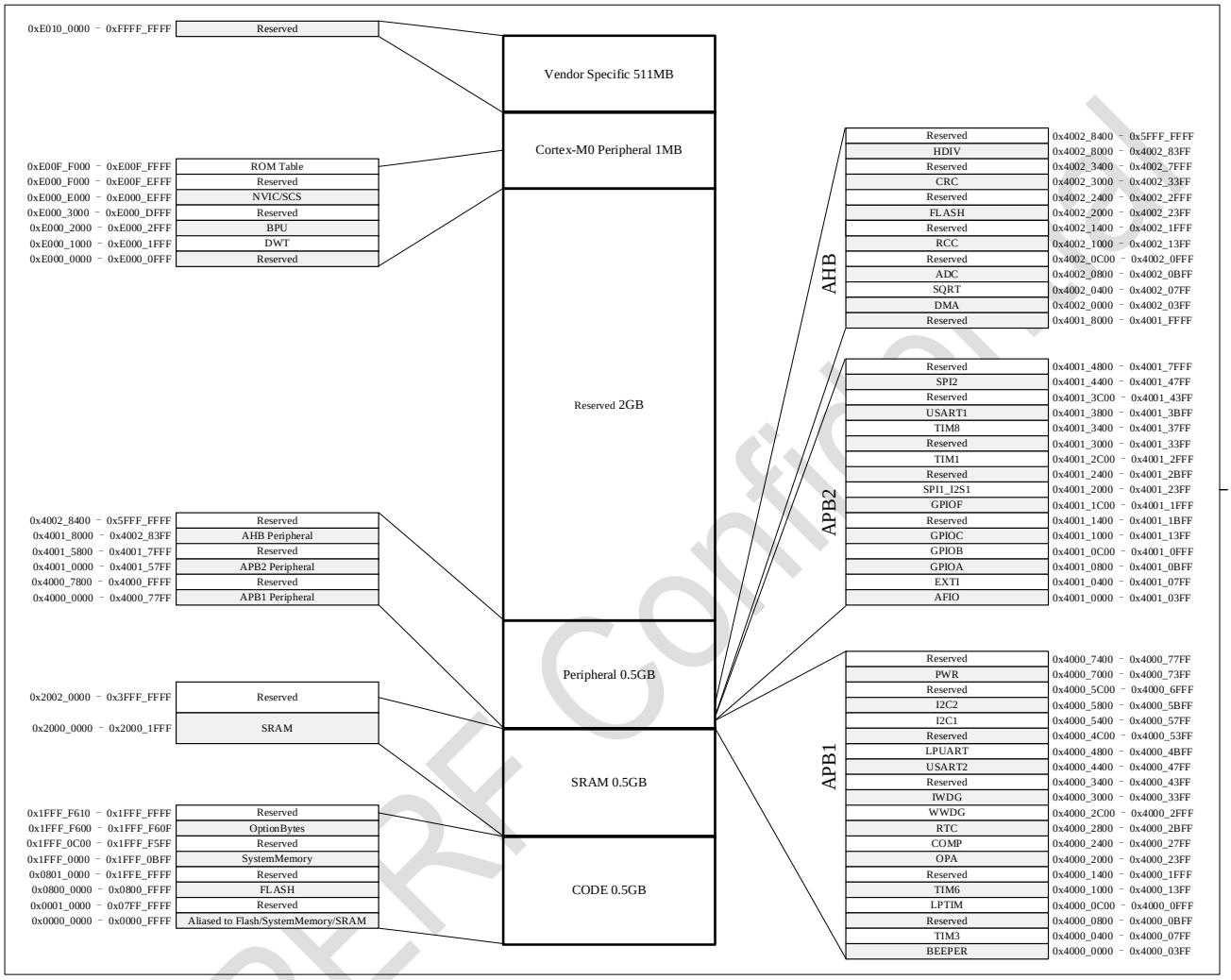


Figure 5-1. Memory Address Map

5.1.1 Embedded Flash Memory

The chip integrates 64 K bytes of embedded flash memory (FLASH) for storing programs and data. The page size is 512 byte and supports page erase, word write, word read, half-word read, and byte read operations. Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operations).

5.1.2 Embedded SRAM

Up to 8 K bytes of built-in SRAM is integrated on-chip, and data can be maintained in the STOP mode.

5.1.3 Nested Vectored Interrupt Controller（NVIC）

The Nested Vectored Interrupt Controller (NVIC) is closely connected to the interface of the processor core, which can realize low-latency interrupt processing and efficiently handle late-arriving interrupts. The nested vectored interrupt controller manages interrupts including kernel exceptions.

- 32 maskable interrupt channels(not including 16 Cortex®-M0 interrupt lines)；
- 4 programmable priority levels (using 2-bit interrupt priority levels)；

- Low-latency exception and interrupt handling；
- Power management control；
- Realization of system control register；

The module provides flexible interrupt management functions with minimal interrupt delay.

5.2 Extended Interrupt/ Event Controller (EXTI)

The extended interrupt/event controller includes 24 edge detection circuits that generate interrupts/event triggers. Each input line can be independently configured as an event or interrupt, as well as three trigger types of rising edge, falling edge or both edges, and can also be independently shielded. The suspend register holds the interrupt request of the status line, and the corresponding bit of the suspend register can be cleared by writing '1'.

5.3 Clock System

The clock of the device includes internal high-speed RC oscillator HSI (8 MHz), internal low-speed clock LSI (30 KHz), external low-speed clock (32.768 KHz), PLL.

The system clock (SYSCLK) can choose the following clock sources:

- HIS oscillator clock
- PLL clock
- LSI oscillator clock
- LSE oscillator clock

2 secondary clock source：

- 30 Khz low-speed internal RC，which can be used as the clock source of IWDG, RTC, LPTIMER and LPUART. Used to automatically wake up the system from STOP mode.
- 32.768 KHz low-speed external crystal can be used as the clock source of RTC、LPTIMER and LPUART.
- When not in use, any clock source can be independently startup or shutdown to reduce system power consumption.

The HSI clock is selected as the default system clock during reset. When needed, it is possible to take safe interrupt management of the PLL clock (for example, when the indirect external oscillator fails).Users can configure the frequency of AHB and APB (APB1 and APB2) domains through multiple prescalers. The maximum allowable frequency of AHB domain, APB 1 domain and APB 2 domain is 48MHz.Figure 5-2 is a clock block diagram tree.

Clock Tree

HSE = High-speed external clock signal(CMT2380F64 not support)
HIS = High-speed internal clock signal
LSE= Low-speed external clock signal
LSI = Low-speed internal clock signal

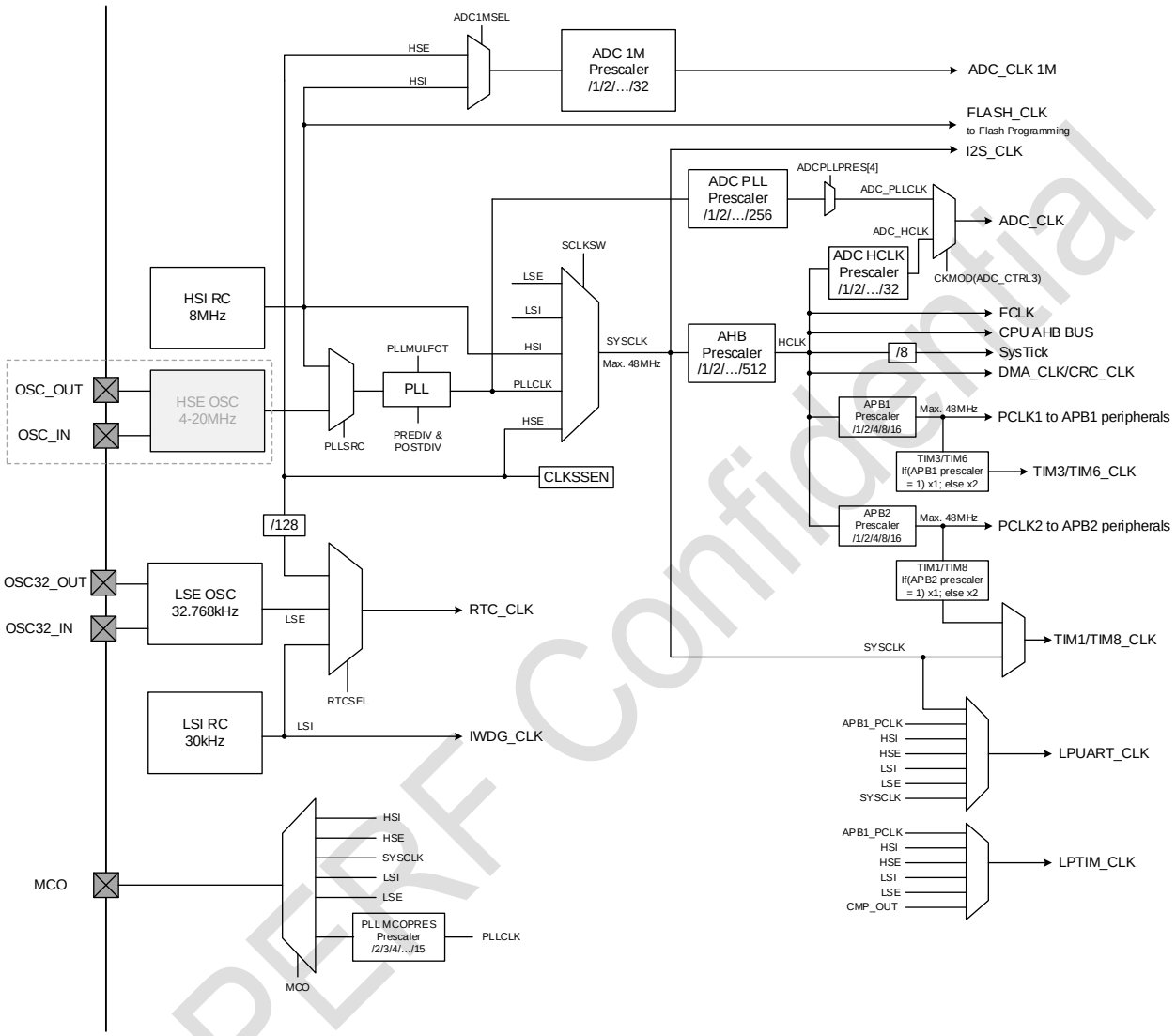


Figure 5-2. Clock Tree

5.4 Boot Modes

At startup, BOOT0 pin and Flash system configuration bits can be selected from one of the three boot options:

- Boot from FLASH Memory
- Boot from System Memory
- Boot from on-chip SRAM

The Bootloader is located in the internal system memory.

5.5 Power Supply Scheme

- VDD area：The voltage input range is 1.8 V~3.6 V，which mainly provides power input for Main Regulator, IO and clock reset system.
- VDDA area：The voltage input range is 1.8 V~3.6 V，which supplies power for most of the external analog peripherals. For more information, please refer to the electrical characteristics section of the relevant data manual.

- VDDD area：The voltage regulator supplies power for CPU, AHB, APB, SRAM, FLASH and most of the digital peripheral interfaces.
- PWR is the power control module of the entire device, its main function is to control CMT2390F64 to enter different power modes and can be awakened by other events or interrupts. CMT2390F64 supports RUN, LPRUN, SLEEP, STOP and PD modes.

5.6 Programmable Voltage Monitor

The power-on reset (POR) and power-down reset (PDR) circuits are integrated internally. This part of the circuit is always in working condition to ensure that the system works normally when the power supply voltage exceeds 1.8 V. When VDD is lower than the set threshold (VPOR/PDR), the device remains in the reset state. The device has a programmable voltage monitor (PVD), which monitors the MCU_VDD/ MCU_VDDA power supply and compares it with the threshold VPVD. When VDD is lower or higher than the threshold VPVD, it will generate an interrupt. The PVD function is turned on by software.

For the values of VPOR/PDR and VPVD, please refer to the table for Embedded Reset and Power Control Module Features

5.7 Low Power Mode

CMT2390F64 is in operation mode after system reset or power-on reset. When the CPU does not need to run(for example, waiting for external events）, users can choose to enter a low-power mode to save power.

CMT2390F64 has the following four low-power modes：

- LPRUN mode（low-power operation mode，the system is in 32.768 KHz low-frequency operation mode）
- SLEEP mode（the core is stopped, all peripherals including Cortex®-M0 core peripherals (such as NVIC, SysTick are still running）
- STOP mode（most of the clocks are turned off, the voltage regulator is still running in low power consumption mode）
- PD mode（VDDD power-down mode，VDD hold，3 WAKEUP IO and NRST can be wake up）
- In addition，the following methods can also reduce the power consumption in RUN mode:
  - Reduce the system clock frequency
  - Turn off the unused peripheral clocks on the APB and AHB buses
  - Optional configuration of PWR_CTRL4.STBFLH in RUN mode allows FLASH to enter deep standby mode; when exiting, the system needs to wait about 10 us before re-accessing FLASH

5.8 Direct Memory Access（DMA）

Integrated 1 general purpose 5-channel DMA controller to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral data transfer; Each channel has a dedicated hardware DMA request logic, and each channel can be triggered by the software. The transmission length of each channel, source address and destination address of transmission can be set separately by software.
DMA can be used for the main peripherals: SPI, I2C, USART, Universal, Basic and Advanced Control Timers TIMx, I2S, ADC.

5.9 Real Time Clock（RTC）

Real Time Clock (RTC) has a set of BCD timers/counters that count independently and continuously. Under the corresponding software configuration, it can provide calendar function. The RTC can also provides two programmable clock interrupts.
Two 32-bit registers contain decimal format (BCD) for subseconds, seconds, minutes, hours (in 12 or 24 hour format), days of the week, days (date), months, and years.
Subsecond values are provided in binary format as separate 32-bit registers. Additional 32-bit registers contain programmable seconds, minutes, hours, days of the week, days, months, and years.
RTC provides automatic wake up in low power mode. When a timestamp function event or intrusion detection event is enabled on GPIO, the current calendar is saved in a register.

5.10 Timer and Watch Dog

CMT2390F64 supports 2 advanced-control timers, 1 general-purpose timer, 1 basic timer and 1 low-power timer, as well as 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced-control timers, general-purpose timers and basic timers:

Table 5-1. Timer Function Comparison

Timer	Counter resolution	Counter type	Prescaler	Generate DMA request	Capture/ Compare channel	Complementary output
TIM1 TIM8	16 bits	Up Down Up/Down	Any integer between 1~65536	support	4	support
TIM3	16 bits	Up Down Up/Down	Any integer between 1~65536	support	4	unsupport
LPTIM	16 bits	Up	2^N, N represents for any integer between 0~7	unsupport	2	unsupport
TIM6	16 bits	Up	Any integer between 1~65536	support	0	unsupport

5.10.1 Basic Timer TIM6

The basic timer (TIM6) contains a 16-bit auto-load counter, driven by a programmable prescaler. It can provide a time base for general-purpose timers.
The main functions of the basic timer are as follows:

- 16 bit automatic reload accumulating counter;
- 16 bit programmable (can be modified in real time) prescaler, used to divide the input clock by coefficient between 1 and 65536;
- Interrupt / DMA request is generated when an update event (counter overflow) occurs.

5.10.2 General Purpose Timer TIM3

CMT2390F64 has a built-in general-purpose timer (TIM3) that can run synchronously. The timer has a 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent channels. Each channel can be used for input capture (for measuring pulse width), output comparison, PWM and single pulse mode output.

The main functions of the general-purpose timer include:

- 16 bit up,down, up/down automatic loading counter;
- 16 bit programmable (can be modified in real time) prescaler, the frequncy division coefficient of the counter clock frequncy is any value between 1～65536;
- 4 independent channels:
  - Input capture;
  - Output comparision;
  - PWM generation (edge or center alignment mode);
  - Single pulse mode output;
- Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected;
- Interrupt /DMA is generated when the following events occur:
- Update: counter overflow/downflow, counter initialization (trigger through software or internal/external);
- Trigger events(counter start, stop, initialization or count by internal/external trigger) ;
- Input capture;
- Output comparision;
- Supports incremental(quadrature) encoder and Hall sensor circuits positioning;
- Trigger input as an external clock or current management by cycle

5.10.3 Low Power Timer (LPTIM)

LPTIM is a 16-bit timer that can work with extremely low power consumption. Thanks to the diversity of clock sources, LPTIM can operate in all power modes except PD mode. Since LPTIM can run without an internal clock source, it can be used as a "pulse counter", which is very useful in some applications. In addition, LPTIM has the ability to wake up the system from low-power consumption mode, which makes it suitable for implementing "timeout function" monitoring with extremely low power consumption.

LPTIM introduces a flexible clock scheme that provides the required functions and performance while minimizing power consumption.

The main functions of low-power timers include:

- 16 bit upward automatic loading counter；
- 3 bit prescaler, 8 kinds of frequency division factors（1、2、4、8、16、32、64、128）；
- Abundant clock source：
  - Internal clock source：HSI，HSE，LSI，LSE，APB1 and CMP_OUT six clock sources；
  - External clock source input through LPTIM（no LP oscillator runs during operation, used for pulse counter applications）；
- 16 bit ARR automatic loading register；
- 16 bit comparator register；
- Continuous or single trigger mode；
- Optional software and hardware input trigger；
- Programmable digital anti-shake filter；
- Configurable IO level polarity；
- Configurable single pulse or PWM output；
- Sopport encoder mode；

5.10.4 Adcanced Control Timer (TIM 1/TIM 8)

Two independent advanced timers (TIM1/TIM8), each timer is composed of a 16-bit auto-loading counter driven by a programmable prescaler. Supports multiple functions, including measuring pulse width of the input signal (input capture), or generating output waveform (output comparison, PWM, complementary PWM outputembedded in dead time, etc.). By using timer prescaler and RCC clock control prescaler, pulse width and waveform period can be adjusted from several microseconds to several milliseconds. Each timer is completelyindependent and does not share any resources with each other.

The main functions of the advanced timer include:

- 16-bit up, down, up/down automatic loading counter
- 16-bit programmable (can be modified in real time) prescaler, the frequency division coefficient of the counter clock frequency is any value between 1 and 65536
- Supports up to 48 Mhz as the timer input clock
- Up to 4 independent channels :
  - Input capture
  - Output comparision
  - PWM generation (edge or center alignment mode)
  - Single pulse mode output
- PWM trigger ADC sampling
- The trigger time point can be configured by software in the entire PWM cycle
- Complementary output with programmable dead time
- Use external signals to control the timer or the synchronization circuit when multiple timers are interconnected
- Allow to update the repeat counter of the timer register after a specified number of counter cycles
- Break input signal can put the timer output signal in a reset state or a known state
- Interrupt/DMA is generated when the following events occur:
  - Update：counter overflow/downflow, counter initialization (through software or internal/ external trigger)
  - Trriger events (counter start, stop, initialization or count by internal/ external trigger)
  - Input capture
  - Output comparision
  - Break signal input
- Supports incremental (quadrature) encoder and Hall sensor circuits for positioning
- Trigger input as an external clock or current management by cycle

In debug mode, the counter can be frozen and the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Many of the functions are the same as the standard TIM timer, and they also have the same internal structure, so the advanced control timer can operate in collaboration with the TIM timer through the timer link function to provide the synchronization or event link function.

5.10.5 Systick

This timer is specific used for real-time operating system and can also be used as a standard decrement counter.
It has the following characteristics:

- 24 bit decrement counter
- Automatic reload function
- A maskable system interrupt can be generated when the counter is 0
- Programmable clock source

5.10.6 Watchdog Timer (WDG)

Two watchdogs are supported, Independent Watchdog (IWDG) and Window Watchdog (WWDG).Two watchdogs provide increased security, timing accuracy and flexibility in use.

- **Independent watchdog（IWDG）**

The independent watchdog is based on a 12-bit decline counter and an 8-bit prescaler, driven by an independent low- speed RC oscillator that remains effective in the event of a master clock failure and operates in STOP mode. Once activated, IWDG generates a reset when the counter counts to 0x000if the dog is not fed within the set time (clearing the watchdog counter). It can be used to reset the entire system in the event of an application problem, or as a free timer to provide timeout management for the application. The option byte can be configured to be software or hardware enabled watchdog. Reset and low power wake-up are available.

- **Window watchdog（WWDG）**

Window watchdogs are usually used to monitor software failures caused by external interference or unforeseen logic conditions that cause the application to deviate from the normal operating sequence. Unless the value of the down counter is refreshed before the T6 bit becomes 0, the watchdog circuit will generate an MCU reset when the preset time period is reached. Before the down counter reaches the window register value, if the 7-bit down counter value (in the control register) is refreshed, an MCU reset will also be generated. This indicates that the down counter needs to be refreshed in a limited time window.

Main features:

- WWDG is driven by the clock after the APB 1 clock is divided;
- Programmable free running decrement counter;
- Conditional reset;
- When the decrement counter value is less than 0x40，(if the watchdog is started) a reset is generated;
- Reset when the decrement counter is reloaded outside the window (if the watchdog is activated);
- If the watchdag is enabled and interrupts are allowed, an early wake-up interrupt (EWI) is generated when the decrements counter equals 0x40, which can be used to reload the counter to aviod a WWDG reset.

5.11 I2C Bus Interface

Two independent I2C bus interfaces that provide multi-host functionality to control all I2C bus specific timing, protocols, mediation, and timing. Supports multiple communication rate modes (up to 1MHz), supports DMA operation, and is compatible with SMBUS 2.0.The I2C module has a variety of uses, including CRC code generation and verification, SMBUS (System Management Bus) and PMBUS (Power Management Bus).

The main functions of I2C interface are described as follows:

- Multi-host function: the module can be used as a master device or a slave device;
- I2C master device function:
  - Generate clock;
  - Generate start and stop signals;
- I2C slave device function:
  - Programmable address detection;
  - The I2C interface supports 7 bit or 10 bit addressing and supports dual slave address response in 7 bit slave mode;
  - Stop bit detection;
- Generate and detect 7 bit /10 bit addresses and broadcast calls;
- Support diferent communication speeds:
  - Standard speed (up to 100 kHz);
  - Fast (up to 400 kHz)；
  - Fast + (up to 1 MHz)；
- Status flag:

- Transmitter/ receiver mode falg;
- Byte end flag;
- I2C bus busy sign;

◆ Error flag:
- Arbitration lost in master mode;
- Response（ACK）error after address/data transmission;
- Misaligned start or stop conditions detected;
- Prohibit overflowing or underflowing when elongating the clock function;

◆ 2 interrupt vectors:
- 1 interrupt for address/data communication successful;
- 1 interrupt for error;

◆ Optional elongated clock feature;
◆ DMA with a single byte cache;
◆ Generate or verify configurable PEC (packet error detection):
- The PEC value can be sent as the last byte in transmission mode
- A PEC error check for the last received byte

◆ SMBus 2.0 compatible
- Low timeout delay for 25 ms clock
- 10 ms master device cumulative clock low expansion time
- 25 ms slave device cumulative clock low expansion time
- Hardware PEC generation/verification with ACK control
- Support for address resolution protocol (ARP)

◆ SMBus compatible

5.12 Universal Synchronous Asynchronous Receiver Transmitter （USART）

In CMT2390F64, three serial transceiver interfaces are integrated, including two universal synchronous/asynchronous transceivers (USART1, USART2) and one universal asynchronous transceiver (LPUART) supporting low power mode operation. These three interfaces provide synchronous/asynchronous communication, support for IrDA SIR ENDEC transport codec, multi-processor communication mode, single-wire semi-duplex communication mode, and LIN master/slave functionality.

The USART 1 and USART 2 interfaces have hardware CTS and RTS signal management, ISO7816 compatible smart card mode and SPI-like communication mode, all interfaces can use DMA operation.

The main features of USART are as follows:

◆ Full-duplex, asynchronous communication;
◆ NRZ standard format;
◆ Fractional baud rate generator system, baud rate programmbale for sending and receiving up to 3M bits/s
◆ Programmbale data word length (8 or 9 bits)
◆ Configurable stop bits, supporting 1 or 2 stop bits
◆ The ability of LIN to send a synchronous break and LIN to detect a slave break. When the USART hardware is configured to LIN, the 13 bit break is generated and the 10/11 bit break is detected
◆ Output the sending clock for step transmission
◆ IRDA SIR encoder/decoder, supports 3/16 bit duration in normal mode
◆ Smart card simulation function
- The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3standard；
- 0.5 and 1.5 stop bits for smart cards；

◆ Single-wire half-duplex communication；
◆ Configurable DMA multi-buffer comminucation, receiving/sending bytes in SRAM with centralized DMA buffer
◆ Separate transmitter and receiver enabling bits
◆ Detection mark
- Receive buffer full
- Send bufffer empty
- End of transmission flag

◆ Check control
- Sending check bit

- Check the received data

- Four error detection flags
  - Overflow error
  - Noise error
  - Frame error
  - Check error
- 10 USART interrupt source with flag
  - CTS change
  - LIN break character detection
  - Tx data register empty
  - Tx complete
  - Receive data register full
  - Bus detected as idle
  - Overflow error
  - Noise error
  - Frame error
  - Check error
- Multi-processor communication, if the address does not match, then into silent mode
- Wake up from silent mode (Detect by idle bus or address flag detection)
- There are two ways to wake up the receiver: address bit (MSB. 9th bit), and bus idle
- Mode configuration

USART modes	USART1	USART2	LPUART
Asynchronous mode	√	√	√
Hardware flow control	√	√	√
Multi-cache Communication (DMA)	√	√	√
Multiprocessor communication	√	√	×
Synchronous	√	√	×
Smart card	√	√	×
Half duplex (single wire mode)	√	√	×
IrDA	√	√	×
LIN	√	√	×

5.13 Serial Perigheral Interface（SPI）

Support 2 SPI interfaces, SPI allows the chip to communicate with external devices in half/full duplex, synchronous, serial mode. This interface can be configured to be in master mode and provide a communication clock (SCK) for external slave devices.The interface can also work in a multi-master configuration.It can be used for a variety of purposes, including dual wire simplex synchronous transmission using a two-way data line, and reliable communication using CRC calibration.

The main functions of the SPI interface are as follows:

- Full-duplex synchronous transmission
- Double wire simplex synchronous transmission with or without a third two-way data line
- 8 or 16 bit transmission frame format selection
- Support master mode or slave mode
- Support multi-master mode
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master mode and slave mode: dynamic change of master/slave operation mode
- Programmable clock polarity and phase；
- Programmable data order, MSB before or LSB before；
- Dedicated send and receive flags that trigger interrupts；
- SPI bus busy status flag；
- Hardware CRC to support reliable communication:
  - In send mode, the CRC value can be sent as the last byte；
  - In full duplex mode, CRC check is automatically carried out on the last byte received；

- Main mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffers that support DMA functionality: Generates send and receive requests
- Maximum interface speed: 18Mbps

5.14 Synchronous Serial Interchip Sound（I2S）

I2S is a 4-pin synchronous serial interface communication protocol that can operate in master or slave mode. It can be configured for 16-bit, 24-bit, or 32-bit transmission, as well as input or output channels, and supports audio sampling frequencies from 8 kHz to 96 kHz. It supports four audio standards, including the Philips I2S standard, the MSB and LSB alignment standard, and the PCM standard.

It can work in both master and slave modes in half duplex communication. When it is the master device, it provides a clock signal to an external slave device through the interface.

The main functions of I2S interface are as follows:

- Half-duplex communication (only send or receive at the same time);
- Master or slave operation;
- 8-bit linear programmable pre-divider for accurate audio sampling frequency (8kHz to 96kHz);
- The data format can be 16-bit, 24-bit, or 32-bit;
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame);
- Programmable clock polarity (stable state);
- Overflow flag bits in send mode and overflow flag bits in master/slave receive mode;
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel;
- Supported I2S protocols:
  - I2S Philips standard
  - MSB alignment standard (left alignment)
  - LSB alignment standard (right alignment)
  - PCM standard (16-bit channel frames with long or short frame synchronization or 16-bit data framesextended to 32-bit channel frames)
- Data direction is always MSB first;
- Both sending and receiving have DMA capability
- The master clock can be output to external audio devices, fixed frequency is 256xFs (Fs is the audio sampling frequency)

5.15 General Purpose Input/output（GPIO）

GPIO (General Purpose Input/Output) stands for Generic I/O, AFIO (Alternate-Function Input/Output) stands for Multiplexed Function I/O.The chip supports up to 23 GPIOs and is divided into 3 groups (GPIOA/GPIOB/GPIOC), group A has 13 ports per group, group B has 7 ports(among which 4 of them are SPI multiplexing to RF) and group C has 3 ports.GPIO ports share pins with other reusable peripherals, and users can configure them flexibly according to their needs.Each GPIO pin can be independently configured as an output, input, or multiplexed peripheral function port.Except for analog input pins, all other GPIO pins have high current flow capability.

The main characteristics of GPIO are described as follows:

- GPIO ports can be configured separately by the software in the following modes:
  - Input floated
  - Input pull-up
  - Input pull down
  - Analog function
  - Open drain output and up/down can be configured
  - Push-pull output and up/down configurable
  - Push-pull multiplexing function and up/down configurable
  - Open drain multiplexing function and up/down configurable
- Separate bit setting or bit clearing
- All IO support external interrupt functionality
- All IO support low-power mode wake-up, with rising or falling edges configurable
- Sixteen EXITs can be used for SLEEP or STOP mode wake up, and all I/O can be reused as EXTI

- PA 0/ PC 13/ PA 2 three wake-up IO can be used for PD mode wake-up, I/O filtering time is 1us maximum
- Supports software remapping the I/O reusing function
- Support GPIO locking mechanism, reset mode to clear the locked state
- Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half-word or 8-bit byte access is not allowed).

5.16 Analog to Digital Converter（ADC）

12-bit ADC is a high-speed successive approximation analog-to-digital converter. It has up to 6 channels and can measure 6 external and 3 internal signal sources. The A/D conversion of each channel can be executed in single, continuous, scanning or discontinuous mode. The ADC result can be left-aligned or right-aligned stored in the 16-bitdata register; ADC input clock must not exceed 18 MHz.

The main characteristics of ADC are described as follows:

- Support 1 ADC, single-ended input, can measure 12 external and 4 internal signal sources
- Support 12-bit resolution, the highest sampling rate is 1 MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - Only AHB_CLK can be configured as a working clock source, up to 48 MHz
  - PLL can be configured as a sampling clock source, up to 18 MHz, supportfrequency division 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256
  - AHB_CLK can be configured as the sampling clock source, up to 18 MHz, support frequency division 1, 2, 4, 6, 8, 10, 12, 16, 32
  - The timing clock is used for internal timing functions, and the frequency must be configured to 1 MHz.
- Support timer trigger ADC sampling
- Interrupts are generated at the end of conversion, the end of injection conversion, and the occurrence of analog watchdog events
- Single and continuous conversion mode
- Auto scan mode from channel 0 to channel N
- Data alignment with embedded data consistency
- Sampling interval can be programmed separately per channel
- Both rule conversion and injection conversion have external trigger options
- Discontinuous mode
- ADC power supply requirements: 2.4 V to 3.6 V
- ADC input range: 0 ≤ VIN ≤ VDDA
- During regular channel conversion, a DMA request is generated.

5.17 Operational Amplifier（OPAMP）

Built-in an independent operational amplifier with multiple working modes such as external amplification, internal follower and programmable amplifier (PGA) (or both internal amplification and external filtering).

The main functions are as follows:

- Support rail-to-rail input
- OPA linear output range 0.4 V~VDDA-0.4 V
- Can be configured as independent operational amplifier and programmable gain operational amplifier;
- Forward and reverse input multiple selection；
- OPAMP working mode can be configured as:
  - Independent mode (external gain setting)；
  - PGA mode, programmable gain is set to 2X, 4X, 8X, 16X, 32X
  - Follower mode；
- The internally connected ADC channel is used to measure the output signal of the operational amplifier

5.18 Analog Comparator（COMP）

Built-in 1 comparator, which can be used as a separate device (all ports of the comparator are led to I/O), or it can be used in combination with a timer. In motor control applications, it can be used in conjunction with the PWM output from the timer to form a cycle-by-cycle current control.

The main functions of the comparator are as follows:：

- 1 independent comparator COMP, and it is a low-power comparator (can work in LPRUN, SLEEP and STOP modes)
- Built-in a 64-level programmable reference input voltage source VREF
- Support filter clock, filter reset
- Output polarity can be configured high and low
- Hysteresis configuration can be configured without, low, medium, high
- The comparing results can be output to the I/O port or the trigger timer for capturing events, OCREF_CLR events, braking events, and generating interrupts
- Input channel can be multi-selected I/O port, VREF
- It can be equipped with read-only or read-write, and it needs to be reset to unlock when locked
- Support blanking (Blanking), the blanking source can be configured to generate Blanking
- COMP can wake up the system from low power consumption mode by generating an interrupt, and COMP has the ability to wake up the system from STOP
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

5.19 Temperature Sensor（TS）

The temperature sensor generates a voltage that changes linearly with temperature, and the conversion range is between 1.8 V < VDDA < 3.6 V. The temperature sensor is internally connected to the input channel of ADC_IN12 to convert the output of the sensor to a digital value.

5.20 BEEPER

The BEEPER module supports complementary outputs and can generate periodic signals to drive external passive beeper. Used to generate prompt sound or alarm sound.

5.21 HDIV/ SQRT

The divider (HDIV) and square root (SQRT) are mainly used in some scenarios with high requirements for computing energy efficiency, and are used to partially supplement the deficiencies of the microcontroller in computing. The divider and square root calculator can perform division or square root calculation of unsigned 32-bit integers.

The main features of HDIV and SQRT are as follows:

- Only support word operation
- 8 clock cycles to complete an unsigned integer division operation
- 32-bit dividend, 32-bit divisor, output 32-bit quotient and 32-bit remainder
- Divisor is zero warning flag, division operation end flag
- 32-bit unsigned square root integer, 16-bit root root output
- Complete an unsigned integer square root operation in 8 clock cycles
- You can judge whether the calculation is complete by setting the interrupt enable or query the relevant register bits

5.22 Cyclic Redundancy Check Calculation Unit（CRC）

Integrating CRC 32 and CRC 16 functions, the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335- 1 standard, it provides a means to detect flash memory errors. The CRC calculation unit can be used to calculate the signature ofthe software in real time and compare it with the signature generated when the software is linked and generated

The main characteristics of CRC are as follows:

- CRC 16：Support polynomial X16+X15+X2+X0
- CRC 32：Support polynomial X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 +X2 + X +1
- CRC calculation time：4 AHB clock cycles (HCLK)
- The initial value of cyclic redundancy calculation can be configured
- Support DMA mode

5.23 Unique Device ID（UID）

CMT2390F64 have built-in two unique device ID of different lengths, 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory. The information contained in them is programmed at the factory, and is guaranteed to be unique to any micro-controller under any circumstances. User applications or external devices can be read through the CPU or SWD interface and cannot be modified.

The UID is 96 bits, usually used as a serial number or as a password. When programming the flash memory, this unique identification is combined with the software encryption and decryption algorithm to further improve the security ofthe code in the flash memory. It can also be used for activation with security Functional bootloader (Secure Bootloader).

The UCID is 128 bits and complies with the definition of the chip serial number which contains information on chip production and version.

5.24 Serial Wire SWD Debug Port（SWD）

The ARM SWD Interface is embedded.

6 Order Information

Table 6-1.CMT2390F64 Order Information

Type	Description	Package	Packet Option	Operation Condition	MOQ
CMT2390F64-EQR[1]	CMT2390F64, low power consumption Sub - 1GHz RF transceiverSoC	QFN48(6x6)	Make up with disk	1.8 to 3.6 V, - 40 to 85℃	3,000

Remarks:

[1]. “E” represents the extended industrial product grade，with supported temperature range from - 40 to +85 ℃.

“Q” represents package type of QFN 48.

“R” represents the tape and tray type with MOQ as 3,000.

For more information, please refer to official website: www.hoperf.com

For purchasing or pricing requirements, please contact sales@hoperf.com or your local sales representatives.

7 Package Outline

Package information of CMT2390F64 is shown as followed.

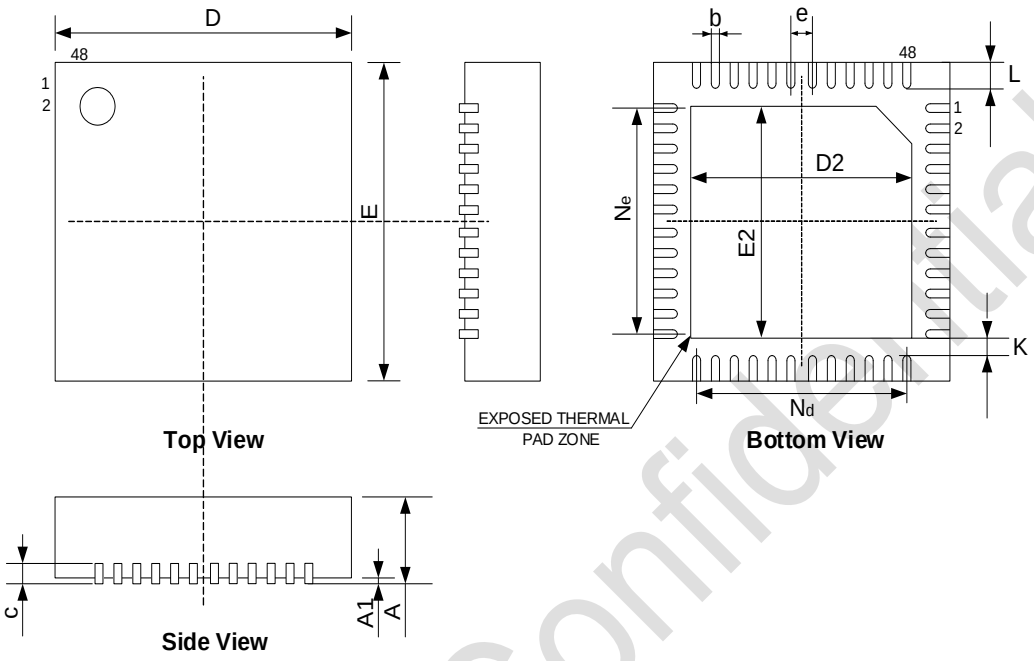


Figure 7-1. QFN48 6x6 Package

Table 7-1. QFN48 6x6 Package Size

Symbol	Size (mm)		
	Min.	Typ.	Max.
A	0.65	0.75	0.85
A1	0	0.02	0.05
A3	——	0.203	——
b	0.175	0.20	0.225
D	5.90	6.00	6.10
E	5.90	6.00	6.10
e		0.40	
D2	——	4.20	——
E2	——	4.20	——
L	——	0.40	——
K	——	0.50	——
R	——	0.05	——

8 Silk Printing Information

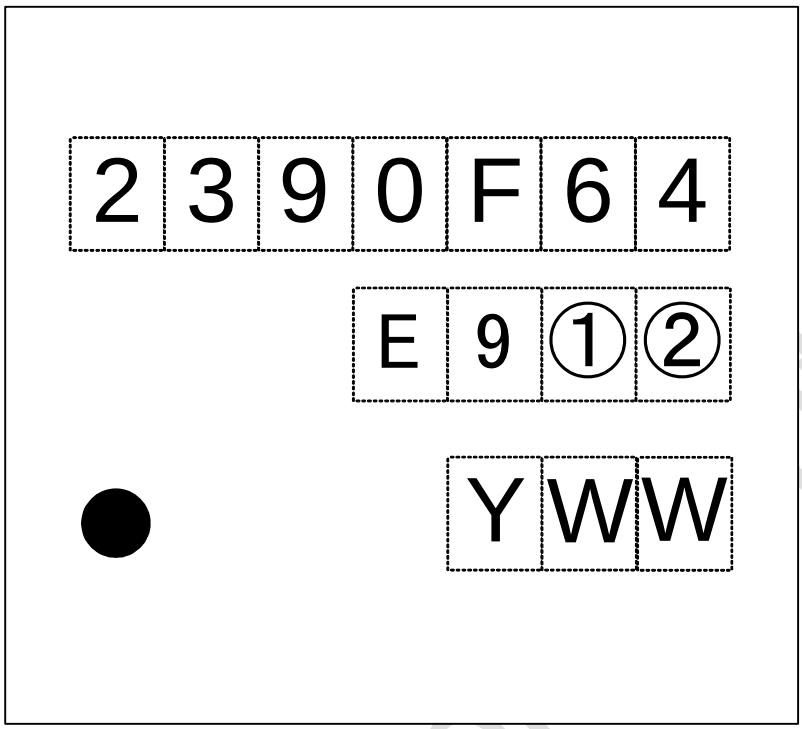


Figure 8-1. CMT2390F64 Top mark

Table 8-1. CMT2390F64 Top Mark Description

Printing method	Laser
Pin1 marking	Circle diameter = 0.3 mm
Font size	0.5 mm, right alignment
First line silk printing	2390F64, Representative model CMT2390F64
Second line silk printing	E9①②Internal tracking code
Third line silk printing	Date code, assigned by packaging plant, Y represents the last digit of the year and WW represents the working week

9 Relevant Documents

Table 9-1. Other Related Application Documents

Number	File Name
AN235	*FIFO and Packet Format Usage Guide*
AN236	*Register Description*
AN237	*CMT2310A Quick Start Guide*
AN238	*CMT2310A RF Parameter Configuration Guide*
AN239	*Using Guide for CMT2310A Auto-transceiver Function*
AN241	*CMT2310A-EB Evaluation Board Operation Guide*

10 Revise History

Table 10-1. Revise History

Version	Chapter	Modify	Date
0.1	All	Initial	2023-01-03
0.2	1.4	Change the Unit of Co-channel rejection，Adjacent channel rejection，Blocking，Image Rejection from dBc to dB.	2023-05-24

11 Contacts

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